BME 373 Electronics II
Electronics II Quiz #1

1. MOSFET Load-line Analysis (20%)
   a. Determine the gain for $V_{GG} = 2, 3, 4, 5$ volts
   b. Which value of $V_{GG}$ produces the best amplifier design? Why? In your answer, include reasons which do NOT only depend upon gain.

\[ V_{in} = 1\sin 20\pi t \]

\[ V_{GG} \]

\[ 15k \]

\[ V_{DD} = 21.5V \]

\[ Id(mAmps) \]

\[ Vds(Volts) \]
Electronics II Quiz #1

2. FET small signal equivalent circuits (45%)
   a. Calculate the value of the gain $\frac{V_{out}}{V_s}$

   - Recall: $I_D = K (V_{GS} - V_{to})^2$ for saturation
   - $g_m = \frac{dI_D}{dV_{GS}} \mid_{Qpoint}$
   - $K_1 = 5 \text{mA/V}^2$, $K_2 = 7 \text{mA/V}^2$
   - $V_{to} = 1V$

   ![Circuit Diagram]
Electronics II Quiz #1

3. What is the value $V_1$, $V_2$, $V_3$, $V_4$ and the voltage from drain to source, $V_{DS}$, for each JFET. (10%)

Assume that the zero bias saturation current for these JFETs is 5mA and $V_{to}$ is -1 volts. Note that $V_1$, $V_2$, $V_3$, and $V_4$ are referenced to ground. Show all work. You may need to use some engineering judgement to solve this problem. Prove your solution.
Electronics II Quiz 1

4. Find the **INVERSE** of these logic expressions (i.e., the logical NOT of $F$). Simply your answer (e.g., using DeMorgan’s Laws) and use truth tables prove your answer. Show all work. Your answer should result in the minimum number of OR gates. (15%)

$$a) F = \overline{A(B + C)} + D$$

$$b) F = \overline{ABC} + A(B + \overline{C})$$

5. Design a logic gate family which sinks to its load

a) Find the max output current for a gate which fans out to support 10 gates. Assume each gate requires an input current of 5 mA. How many gates can be fanned out when the gate maximum output current is 42 mA?

b) Are these current for when the output voltage is High or Low?

c) For this family we are given $V_{IL} = 3 \, V$, $V_{IH} = 2.5 \, V$, $V_{OL} = 1 \, V$, $V_{OH} = 2.5 \, V$, will this Gate operate such that 0s and 1s will be detected properly? (Show the voltage output vs input diagram with the noise margins.) If not, provide a solution with a noise margin of 1 volt for both the High and Low logic levels and a buffer of 1 volt between High and Low. What is the voltage buffer between the worse case High and Low logic levels. (10%)
1. MOSFET Load-line Analysis
   a. Determine the gain for $V_{GG} = 2, 3, 4, 5$ volts
   b. Which value of $V_{GG}$ produces the best amplifier design? Why? In your answer, include reasons which do NOT depend on gain.

\[
\begin{align*}
V_{GG} &= \sin 20\pi t \\
V_{in} &= \sin 20\pi t \\
15k &
\end{align*}
\]

\[
\begin{align*}
V_{in} &= \sin 20\pi t \\
V_{DD} &= 21.5V \\
V_{GS} &= 6 \\
V_{DS} &= 15k \\
R_{D} &= \frac{21.5}{15000} = 1.43mA
\end{align*}
\]
Electronics II Quiz #1

2. FET small signal equivalent circuits (35%)
   a. Calculate the value of the gain $\frac{V_{out}}{V_{s}}$
      
      - Recall: $I_D = K (V_{GS} - V_{to})^2$ for saturation
        $g_m = \frac{dI_D}{dV_{GS}} |_{Q\text{point}}$
        $K_1 = 5 \text{mA/V}^2 \quad K_2 = 7 \text{mA/V}^2$
        $V_{to} = 1V$

      ![FET circuit diagram]

      $V_{DD} = 30$
      $V_{in} = 500$
      $R_L = 1k$
      $R_D = 2k$
      $R_2 = 150k$
      $R_s = 10k$
      $R_i = 300k$
      $R_{in} = 150k$
Electronics II Quiz #1

2. FET small signal equivalent circuits

a. Calculate the value of $R_2$ to yield a value of $V_{GSQ} = 1.75\, V$

b. Calculate the value of the gain $\frac{V_{out}}{V_s}$

- Recall: $I_D = K (V_{GS} - V_{to})^2$ for saturation
  
  $g_m = \frac{dI_D}{dV_{GS}}|_{Q\text{point}}$
  
  $K_1 = 5\, mA/V^2$
  
  $V_{to} = 1\, V$

\[
R_1 = 150\, k\Omega
\]

\[
R_2 = 150\, k\Omega
\]

\[
R_S = 10\, k\Omega
\]

\[
V_{DD} = 30\, V
\]

\[
V_{DS} = 5\, V
\]

\[
V_T = 1.52\, V
\]

\[
V_{GS} = 0.46\, V
\]

\[
I_D = 5\, mA
\]

\[
g_m = 5.2\, mS
\]

DC ANALYSIS FOR BOTH STAGES

\[
V_T = \frac{V_{DD}}{R_1 + R_2} = 15
\]

\[
V_T = V_{GS} + I_D R_S
\]

\[
I_D = K(V_{GS} - V_{to})^2
\]

\[
V_T = V_{GS} + K(V_{GS} - V_{to})^2 R_S
\]

\[
0 = K R_S V_{GS}^2 + (1 - 2KR_S V_{to}) V_{GS} + KR_S V_{to}^2 - V_T
\]

\[
0 = 50V_{GS}^2 - 99V_{GS} + 35
\]

\[
V_{GS} = 0.46, 1.52 \Rightarrow 1.52
\]

\[
I_D = K(V_{GS} - V_{to})^2 = 5m(1.52 - 1)^2 = 1.35\, mA
\]

\[
V_{DS} = V_{DD} - I_D (R_S + R_D) = 30 - 1.33m(10k + 2K) = 13.8\, \text{volts}
\]

\[
g_m = 2K(V_{GS} - V_{to}) = 5.2\, mS
\]
Electronics II Quiz #1

2. FET small signal equivalent circuits
   a. Calculate the value of $R_2$ to yield a value of $V_{GSQ} = 1.75\text{v}$
   b. Calculate the value of the gain $V_{out} / V_s$

   - Recall: $I_D = K (V_{GS} - V_{to})^2$ for saturation
     
     $g_m = dI_D / dV_{GS} |_{Q\text{point}}$
     
     $K_1 = 7\text{mA/V}^2$
     
     $V_{to} = 1\text{V}$
     
     $V_{DD} = 30\text{V}$
     
     $R_2 = 150\text{k}$
     
     $R_1 = 300\text{k}$
     
     $R_D = 2\text{k}$
     
     $R_S = 10\text{k}$

DC ANALYSIS FOR BOTH STAGES

$V_T = V_{DD} + \frac{R_2}{R_4 + R_2} = 10$  
$V_T = V_{GS} + I_D R_S$

$I_D = K (V_{GS} - V_{to})^2$

$V_T = V_{GS} + K (V_{GS} - V_{to})^2 R_S$

$0 = K R_3 V_{GS}^2 + (1 - 2 K R_3 V_{to}) V_{GS} + K R_3 V_{to}^2 - V_T$

$0 = 70 V_{GS}^2 - 1.99 V_{GS} + 60$

$V_{GS} = 0.06, 1.35 \Rightarrow 1.35$

$I_D = K (V_{GS} - V_{to})^2 = 7 m (1.35 - 1)^2 = 0.087\text{mA}$

$V_{DS} = V_{DD} - I_D (R_S + R_D) = 30 - 0.87 m (10k + 2K) = 19.6\text{volts}$

$g_m = 2 K (V_{GS} - V_{to}) = 4.9\text{mS}$
2. FET small signal equivalent circuits

\[ R_{L2}' = R_L \parallel R_{D2} = 667 \]
\[ \frac{V_o}{v_{g2}} = -g_{m2}R_{L2}' = -3.28 \]
\[ R_{L1}' = R_1 \parallel R_2 \parallel R_{D1} = 1.96k \]
\[ \frac{v_{g2}}{v_{g1}} = -g_{m1}R_{L1}' = -10.2 \]
\[ \frac{v_{g1}}{v_s} = \frac{R_1 \parallel R_2}{R_1 \parallel R_2 + R_m} = \frac{75k}{75k + 0.5k} = 0.993 \]
\[ \frac{V_o}{v_s} = \frac{v_o \times v_{g2} \times v_{g1}}{v_{g2} \times v_{g1} \times v_s} = \left( -g_mR_{L2}' \right) \times \left( -g_mR_{L1}' \right) \times \frac{R_1 \parallel R_2}{R_1 \parallel R_2 + R_m} = 33.2 \]
Electronics II Quiz 1

3. What is the value \( V_1, V_2, V_3, V_4 \) and the voltage from drain to source, \( V_{DS} \), for each JFET? \((10\%)\)

Assume that the zero bias saturation current for these JFETs is 5mA and \( V_{to} \) is -1 volts. Note that \( V_1, V_2, V_3, \) and \( V_4 \) are referenced to ground. Show all work. You may need to use some engineering judgement to solve this problem. Prove your solution.

\[ J_1 \text{ and } J_4 \text{ In Saturation: } v_{GS1} = v_{GS4} = 0, I_1 = I_{DSS} = 5mA \]

\[ V_1 = 15 - 5mA \times 300 = 15 - 1.5 = 13.5V \]

Assume symmetry between \( J_2 \) and \( J_3 \) and therefore, \( I_2 = I_3 = 2.5ma\).

\[ K = \frac{I_{DSS}}{V_{to}} = \frac{5 \times 10^{-3}}{1} = 5mA/V^2; \quad V_{to} = -1, \quad I_2 = K(v_{GS5} - V_{to})^2 \]

\[ 2.5mA = 5mA/V^2(v_{GS5} - V_{to})^2, \]

we get \( v_{GS2} = v_{GS3} = -0.29V \)

\[ V_3 = - v_{GS2} = 0.29V \]

\[ V_3 = V_{DS4} + 13.5 - 15 = 0.29 \]

\[ V_4 = -15 \]

\[ V_{DS4} = 0.29 + 15 = 15.3V \]

\[ V_{1} - V_{3} = V_{DS1} + V_{DS2} = 13.5 - 0.29 = 13.2V \]

Since \( J_1 \) and \( J_2 \) are the same JFETS and are in saturation, assume \( V_{DS1} = V_{DS2} = 13.2/2 = 6.6. \)

\[ V_2 = V_3 + V_{DS2} = 0.29 + 6.6 = 6.9V \]

Total voltage = 30V = 1.5 + \( V_{DS1} + V_{DS2} + V_{DS4} = 1.5 + 13.2 + 15.3 \text{ QED} \]
4. Use DeMorgan’s Law to find the **inverse** of these logic expressions (i.e., $F$).

\[ a) \overline{F} = \overline{A(B + C) + D} \]
\[ = (A(B + C))D \]
\[ = (A + (B + C))D \]
\[ = (A + (BC))D \]
\[ = AD + BCD \]
4. Use DeMorgan’s Law to find the INVERSE of these logic expressions (i.e., $F$).

\[ b) \overline{F} = \overline{ABC + A(B + C)} = (ABC)'(A(B + C))' = (A + B + C)(A + (B + C)) = (A + B + C)(A + (BC)) = (A + B + C)(A + (BC)) = A(A + (BC)) + B(A + (BC)) + C(A + (BC)) = AA + ABC + B(A + B)BC + CA + CBC = \overline{ABC} + BA + CA \]
Electronics II Quiz 1

5. Design a logic gate family which sinks to its load whose
   a) Find the max output current for a gate which fans out to support 10 gates. Assume each gate requires an input current of 5 mA. How many gates can be fanned out when the gate maximum output current is 42 mA?
   b) Are these current for when the output voltage is High or Low?

   \[ I_I = 5mA; N = 10 \]
   \[ I_O = N \times I_I = 10 \times 5mA = 50mA \]
   \[ 42mA / 5mA = 8.4 \text{ or } 8 \text{ gates} \]
   b) When the gate sinks, current flows to the load when the output voltage is low.
Electronics II Quiz 1

c) For this family we are given \( V_{IL} = 3\, V, \, V_{IH} = 2.5\, V, \) \( V_{OL} = 1\, V, \, V_{OH} = 2.5\, V, \) will this Gate operate such that 0s and 1s will be detected properly? (Show the voltage output vs input diagram with the noise margins.) If not, provide a solution with a noise margin of 1 volt for both the High and Low logic levels and a buffer of 1 volt between High and Low. What is the voltage buffer between the worse case High and Low logic levels.

Since \( V_{OH} \) less then \( V_{IH} \) will cause errors since output which may be considered to be one (e.g., \( V_{OUT} = 2.75 > V_{OH} \)) will be considered and error since \( V_{OUT} \) is less than \( V_{IH} \).

Make \( V_{IL} < V_{OH} \) to operate properly. \( NM_H = V_{OH} - V_{IH} \) and \( NM_L = V_{IL} - V_{OL} \)

Buffer = 3 – 2 = 1 volts