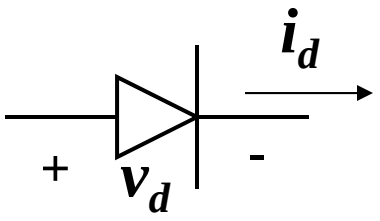
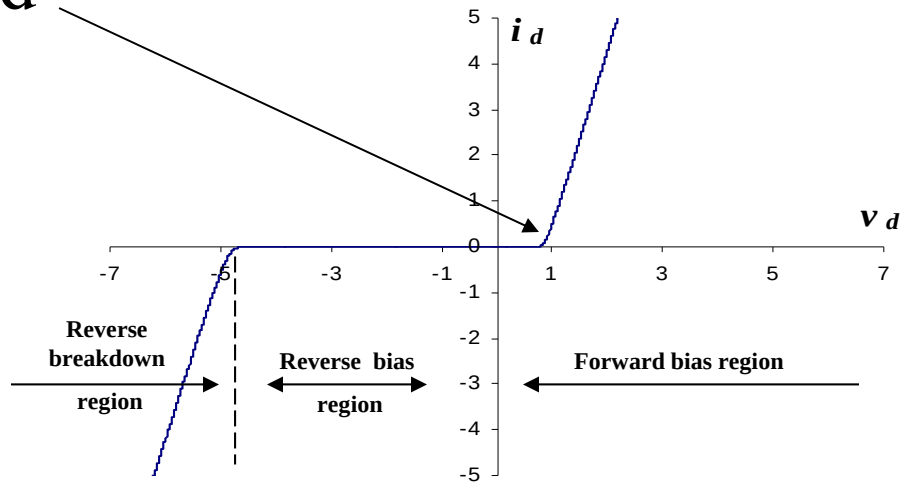
Diodes

Lesson #6
Chapter 3

Diodes

- Typical Diode VI Characteristics
  - Forward Bias Region
  - Reverse Bias Region
  - Reverse Breakdown Region
  - Forward bias Threshold

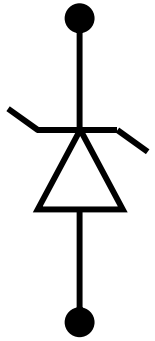




VI stands for Voltage Current

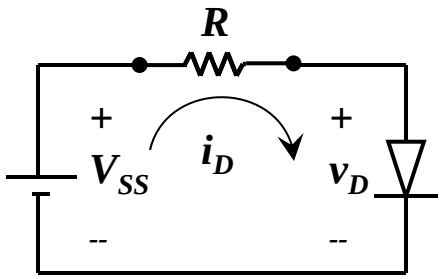
Zener Diodes

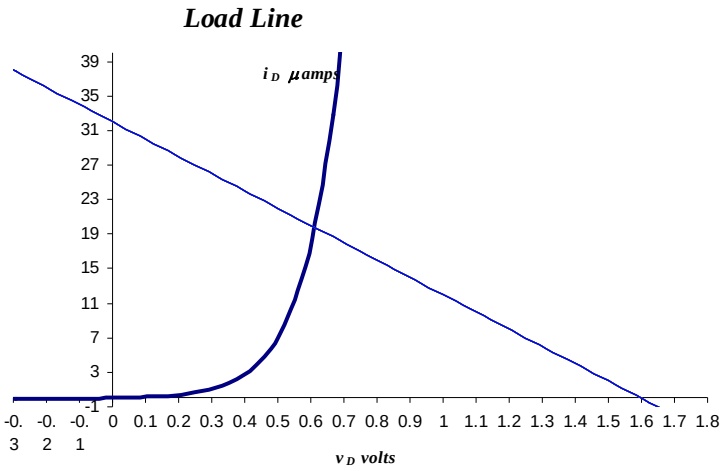
- Operated in the breakdown region.
- Used for maintain a constant output voltage



Load Line Analysis

- Let's see how to use a diode in a circuit.





- Use KVL for this circuit

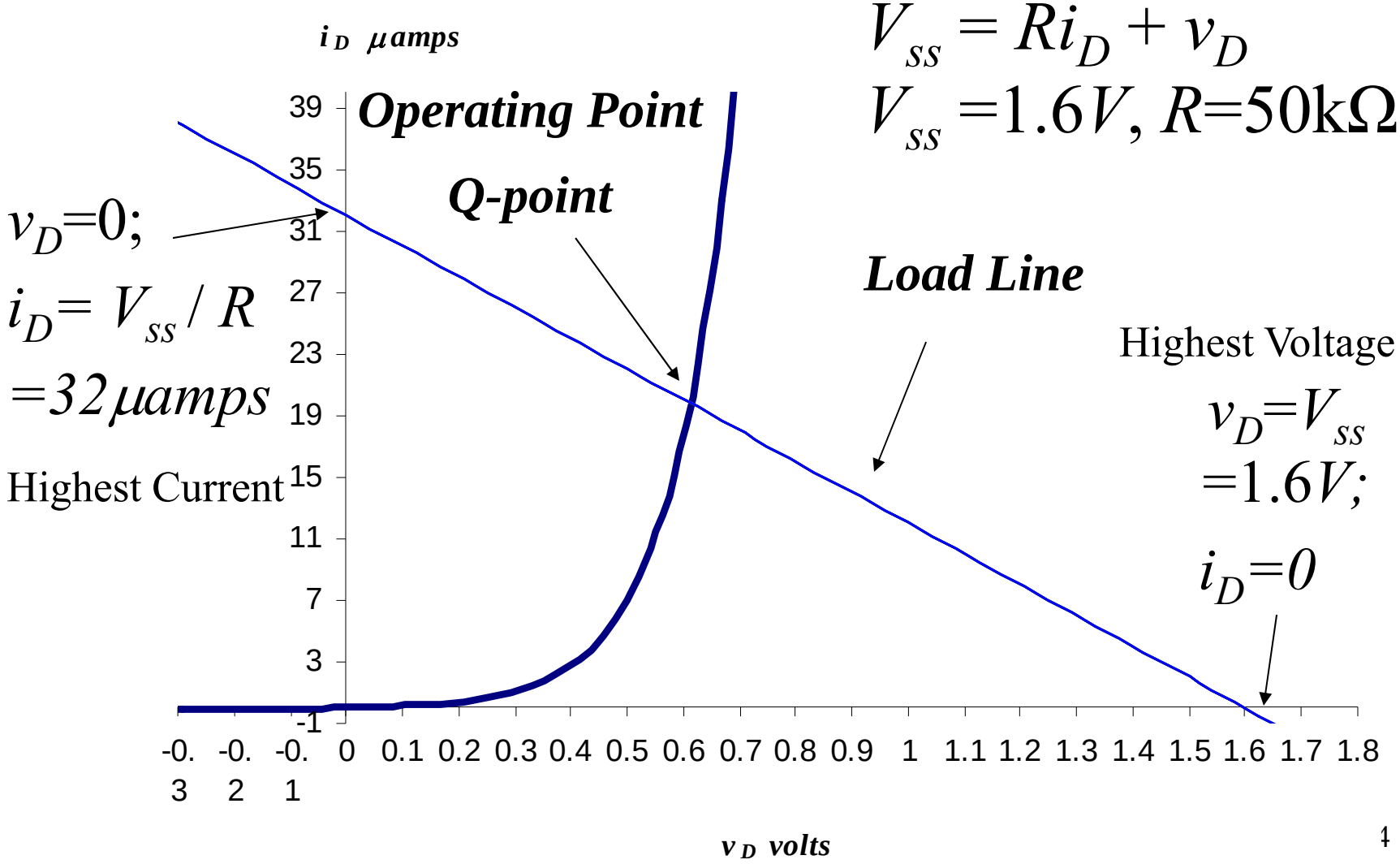
$$V_{ss} = Ri_D + v_D$$

- This equation is plotted on the same graph as the diode VI characteristics.

Load Line Analysis

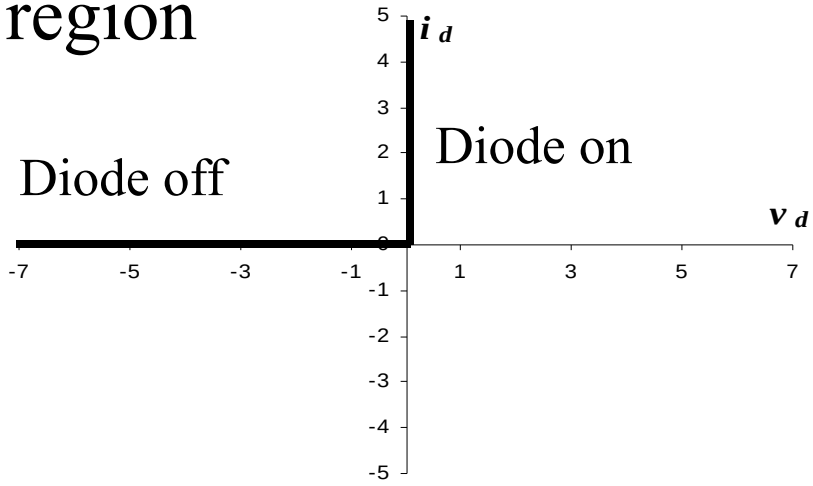
$V_{ss} = Ri_D + v_D$

$V_{ss} = 1.6V,\ R = 50\text{k}\Omega$



Ideal Diode

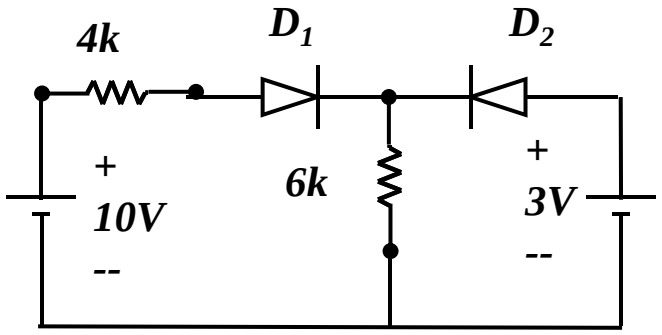
- Basically, a switch
  - Forward Bias: any current allowed, diode on
  - Reverse Bias: zero current, diode off
  - No reverse breakdown region

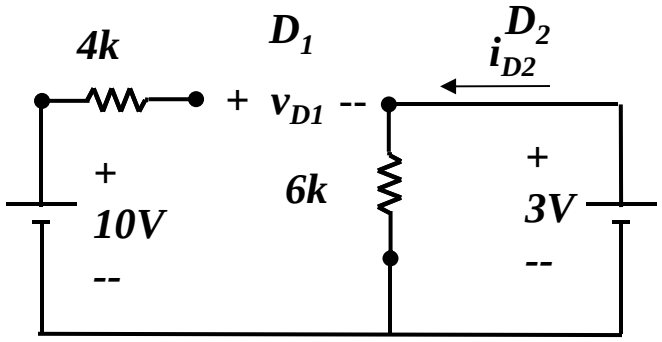


How do we Analysis a Circuit with an Ideal Diode

- For a real diode we use load line (graphical analysis)
- For an ideal diode, we use a deductive method:
  1. Assume a set of states for the diodes
  2. Solve the circuit to find the currents, i_D, of diodes assumed to ON and the voltages, v_D, of the diodes assume to be OFF
  3. Check to see if i_D is positive for all diodes assumed to be ON and v_D is negative for all diodes assumed to be OFF
  4. If this is true, then the solution is complete; otherwise return to step 1 by assuming a different set of states for the diodes.

Example



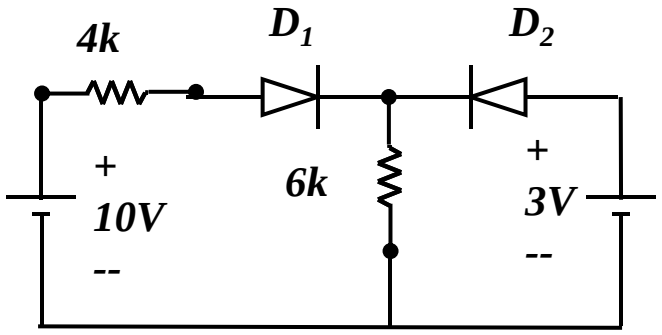


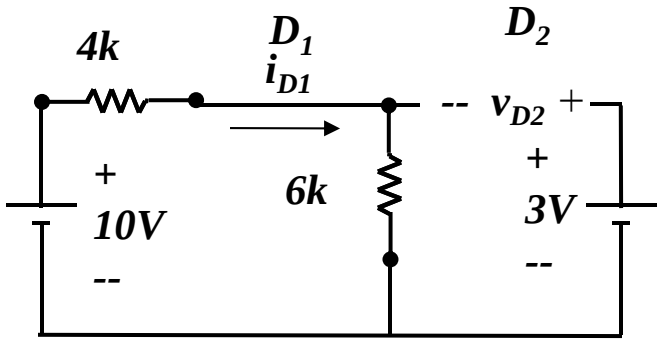
1. Assume D1 OFF and D2 ON
2. Solve the circuit to find the currents, i_D, of diodes assumed to ON and the voltages, v_D, of the diodes assume to be OFF

   i_{D2} = 3/6k = 0.5mA OK **POSITIVE**

   v_{D1} = 10 - 3 = 7 V ***NOT OK*** SHOULD BE ***NEGATIVE***
3. NEED TO START OVER WITH ANOTHER ASSUMPTION

Example





1. Assume D1 ON and D2 OFF
2. Solve the circuit to find the currents, i_D, of diodes assumed to ON and the voltages, v_D, of the diodes assume to be OFF

   i_{D1} = 10/10k = 1mA OK **POSITIVE**

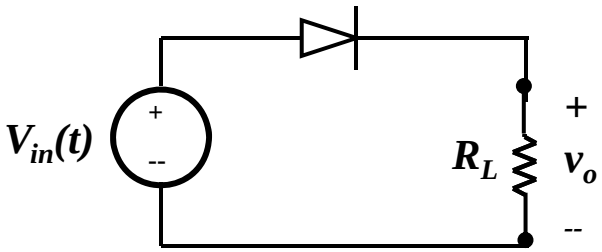
   v_{D2} = 3 - 6 = -3 V OK **NEGATIVE**
3. SOLUTION FOUND!!!!

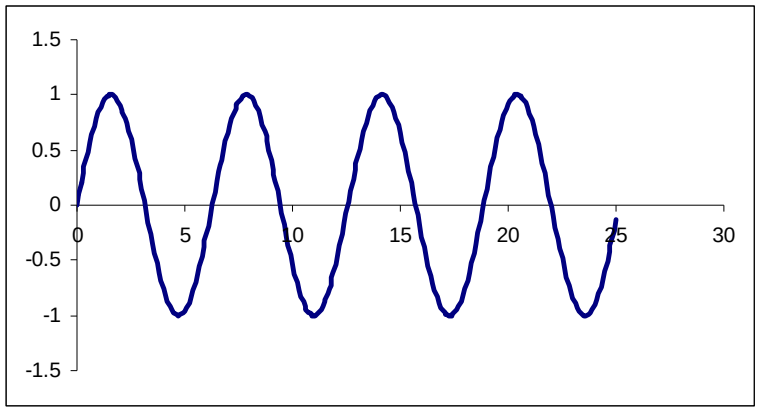
How Do We Use Diodes

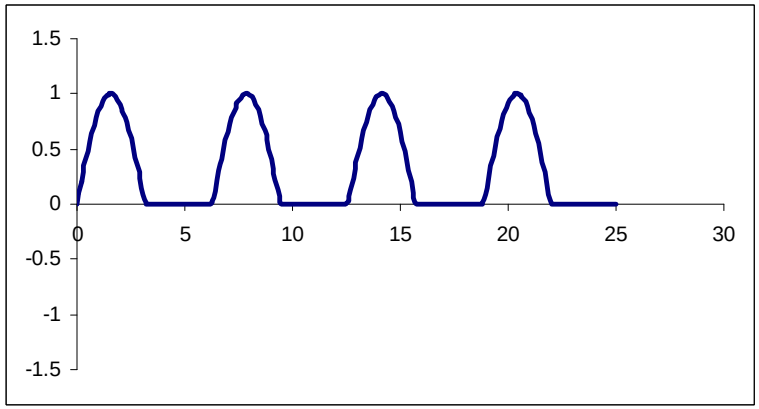
- Rectifier circuits
  - Half-wave: only one (positive or negative) side of a waveform is passed
  - Full-wave: waveform is made single sided
- Wave Shaping
  - Clipping Circuits: waveforms are limited in amplitude
  - Clamping Circuits: the extreme values of a waveform is clamped to a set value
- Logic Circuits
  - AND and OR gates
- Voltage Regulators

Rectifier Circuits

- Half Wave Rectifier
  $V_{in}(t) = V_m \sin(\omega t)$

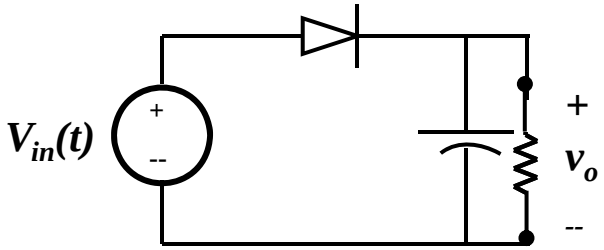


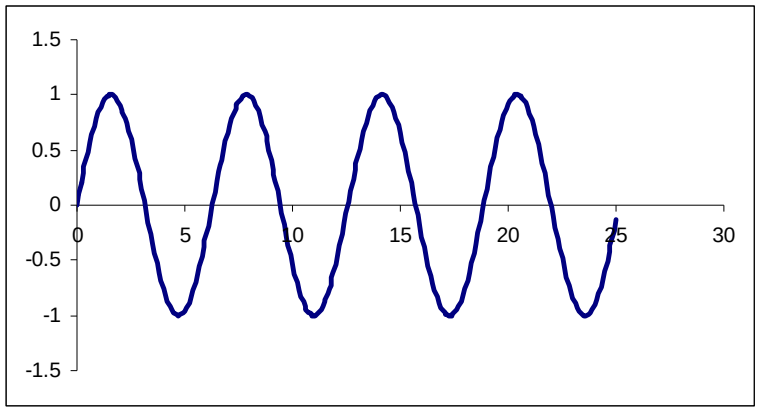


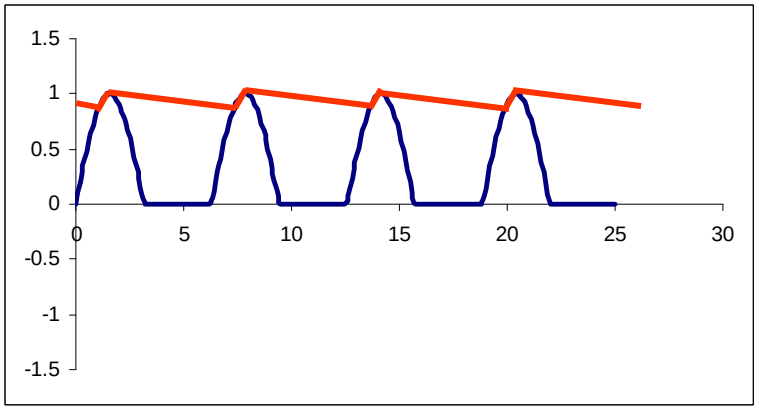


Rectifier Circuits

- Half Wave Rectifier with a smoothing Capacitor
- Peak Detector
- Envelop Detector

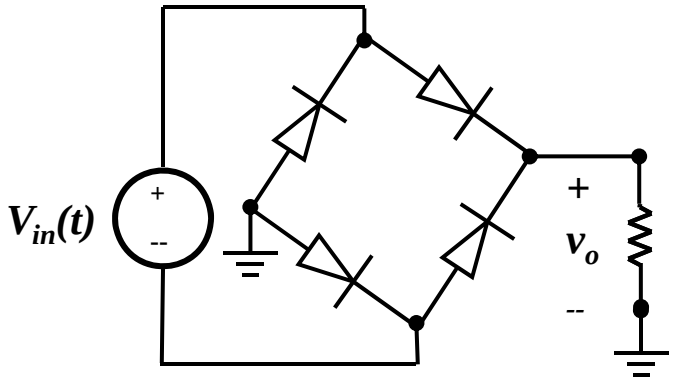


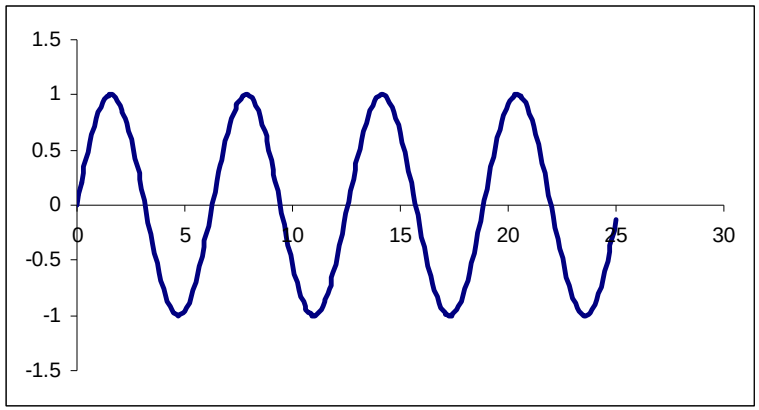


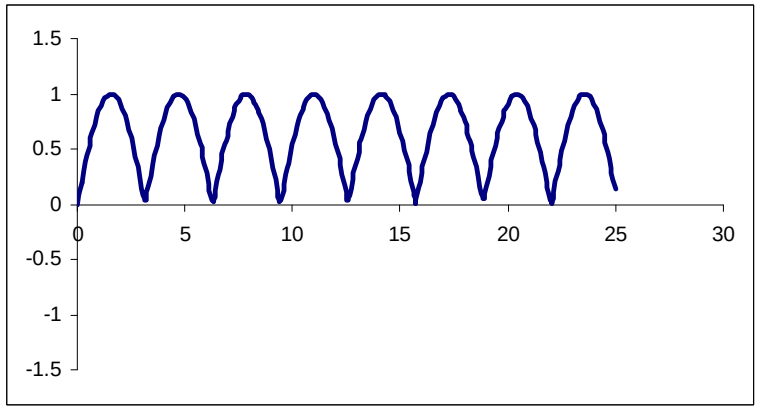


Rectifier Circuits

- Full Wave Rectifier
  $V_{in}(t) = V_m \sin(\omega t)$



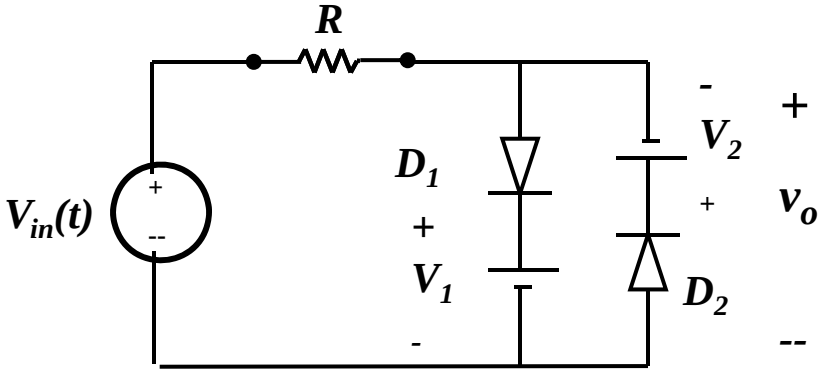


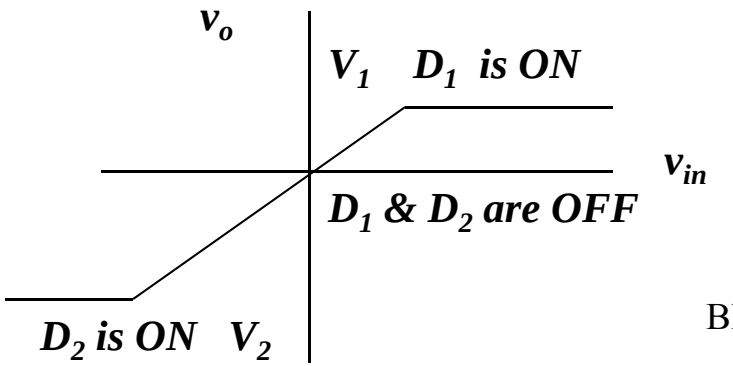


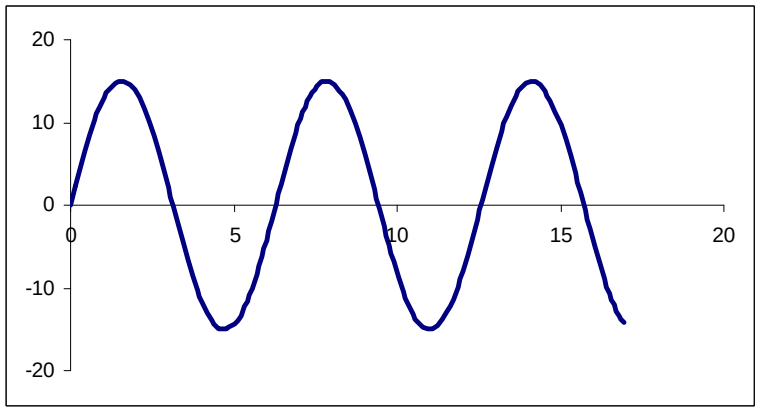
Wave Shaping Circuits

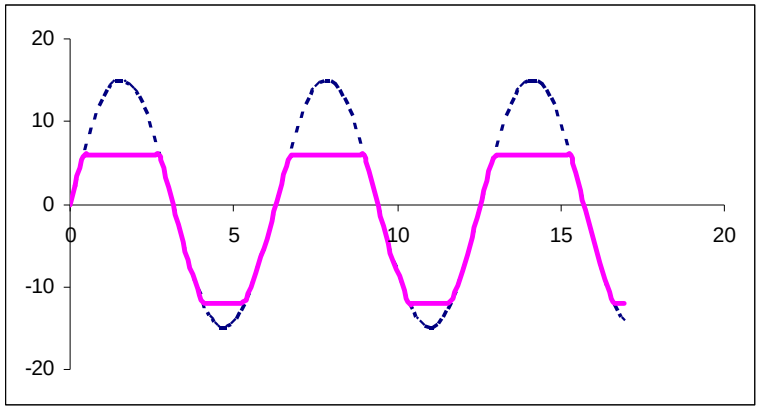
- Clipper Circuits

$$V_{in}(t) = V_m \sin(\omega t)$$





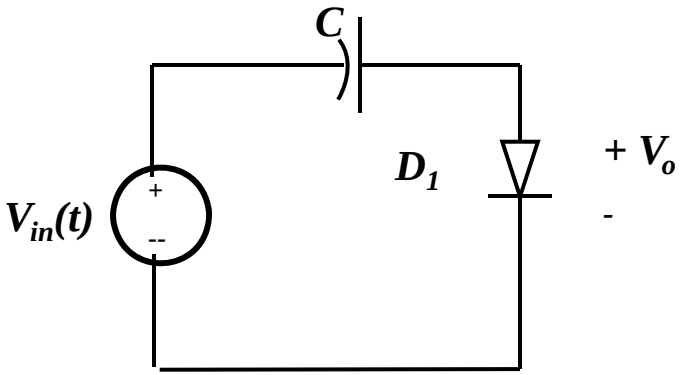


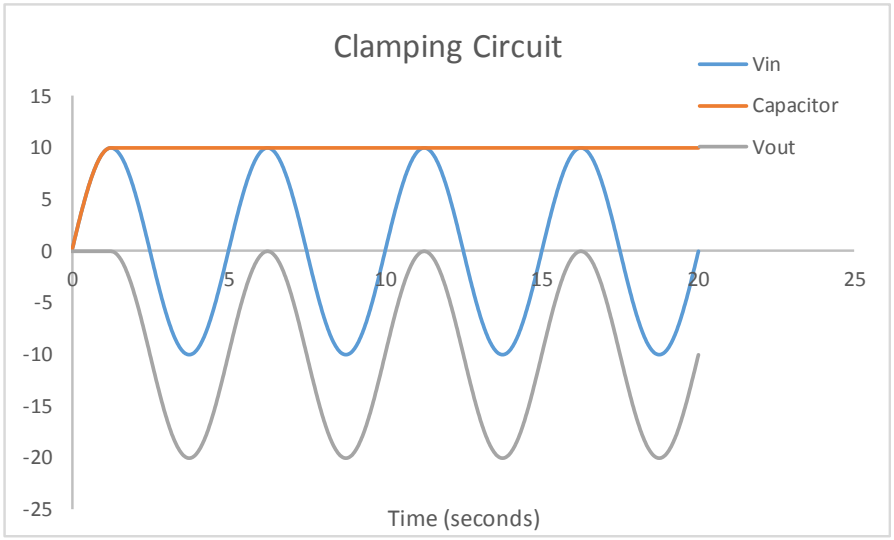


Clamping Circuit

- Clamping Circuits

$$V_{in}(t) = V_m \sin(\omega t)$$





$$V_o(t) = v_d = V_{in}(t) - V_C$$

Note V_C charges *to* V_M

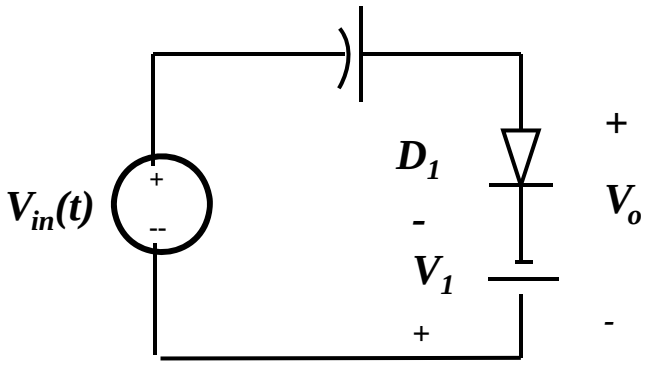
$$V_o(t) = v_d = V_m \sin(\omega t) - V_m$$

- Note at $t = 0$, the voltage across the capacitor is zero and when the diode is forward biased, the capacitor charges up to V_m during the time the diode conducts which is when $V_{in}(t) > 0$
- Thereafter the diode remains reverse biased since $v_d = V_m \sin(\omega t) - V_m$ will never be positive and the capacitor can't discharge and V_o is always < 0

Wave Shaping Circuits

- Clamping Circuits

$$V_{in}(t) = V_m \sin(\omega t)$$



$$V_o(t) = V_{in}(t) - V_C$$

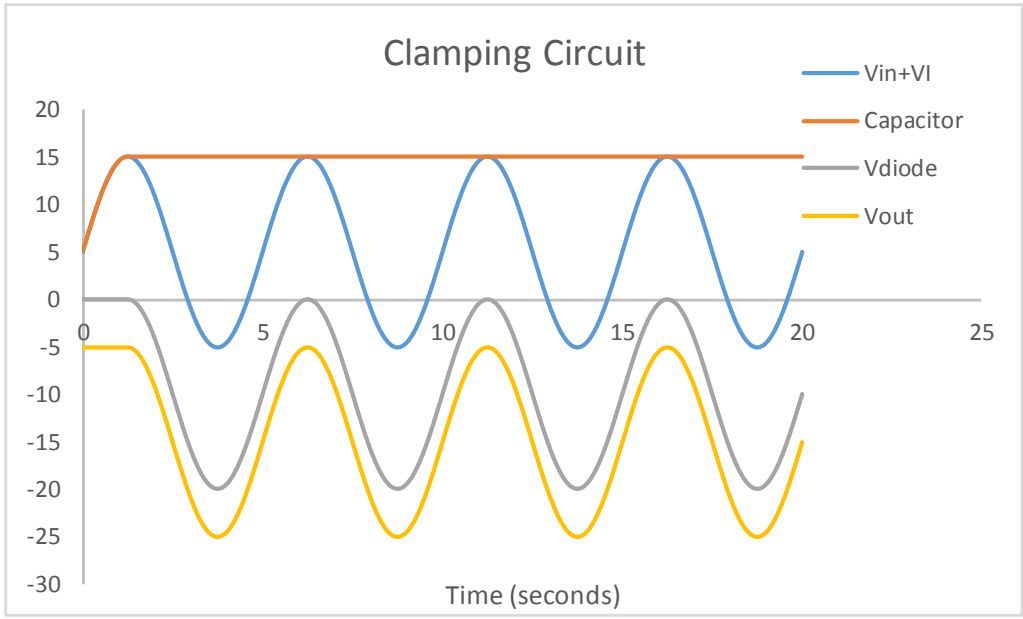
$$v_d = V_{in}(t) - V_C + V_1$$

Note V_C charges *to* $V_M + V_1$

$$V_o(t) = V_m \sin(\omega t) - (V_m + V_1)$$

$$v_d = V_m \sin(\omega t) - (V_m + V_1) + V_1$$

$$= V_m \sin(\omega t) - V_m$$

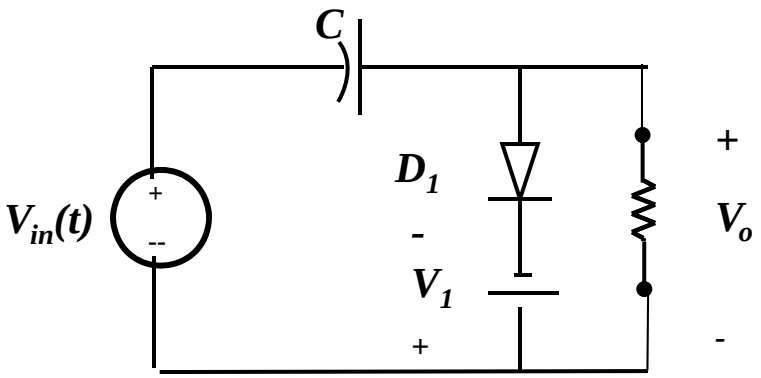


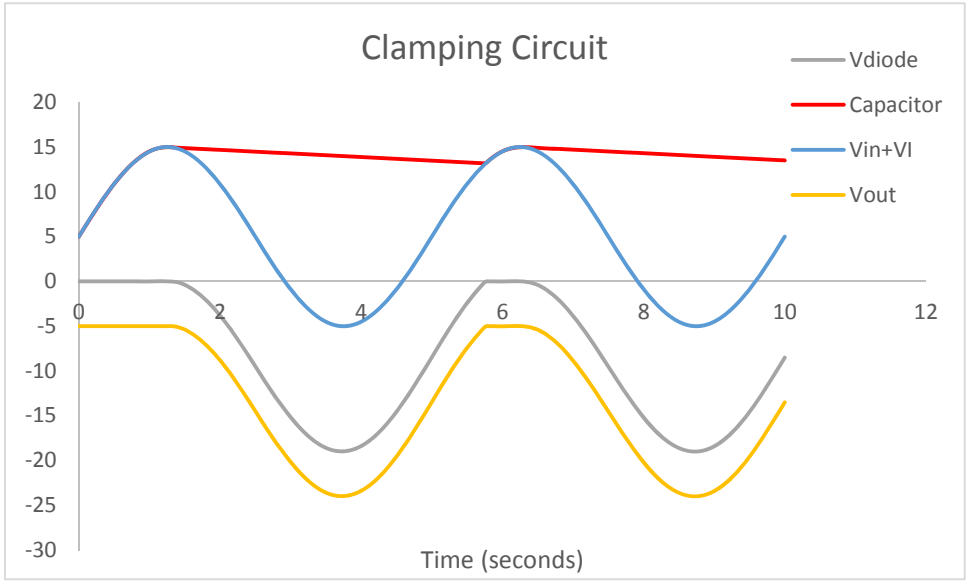
- The capacitor charges up to $V_m + V_1$ during the time the diode conducts which is when $V_{in}(t) + V_1 > 0$
- Thereafter the diode remains reverse biased since $v_d = V_m \sin(\omega t) - V_m$ will never be positive the capacitor can't discharge and V_o is always $< -V_1$

Wave Shaping Circuits

- Clamping Circuits

$$V_{in}(t) = V_m \sin(\omega t)$$





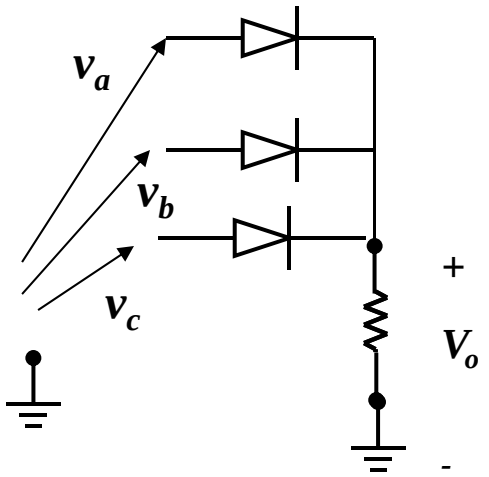
$$V_o(t) = V_{in}(t) - V_C$$

$$V_o(t) = V_m \sin(\omega t) - (V_m + V_1)$$

- A resistor is added to the circuit to allow for changes in input voltage so that the capacitor can discharge if V_{in} drops below V_m

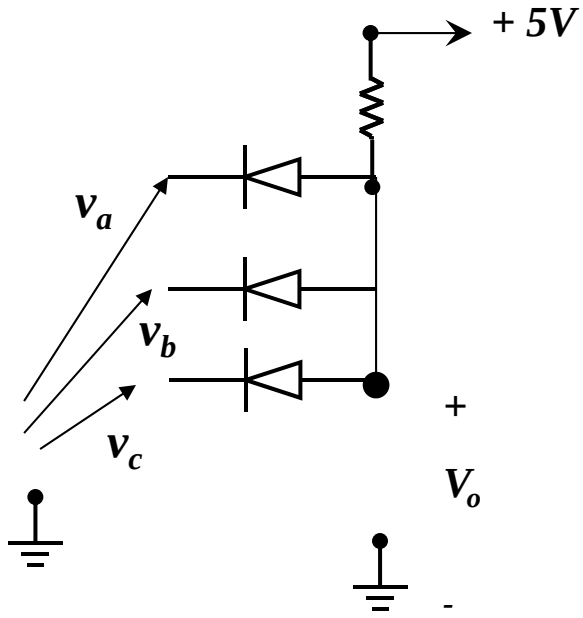
Wave Shaping Circuits

- Logic Circuits
- OR gate



- Output is high when any input is high

- AND gate



- Output high only when all inputs are high

Voltage Regulation

- We want to design a circuit such that its output voltage does not fluctuate due to changes in the load or source.
- Source Regulation: Change in Output voltage due changes in Source Voltage

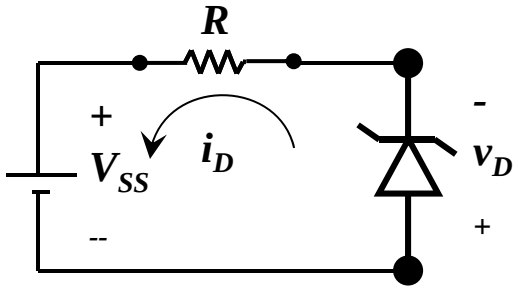
$$\text{Source Regulation} = \frac{\Delta V_{load}}{\Delta V_{SS}} \times 100\%$$

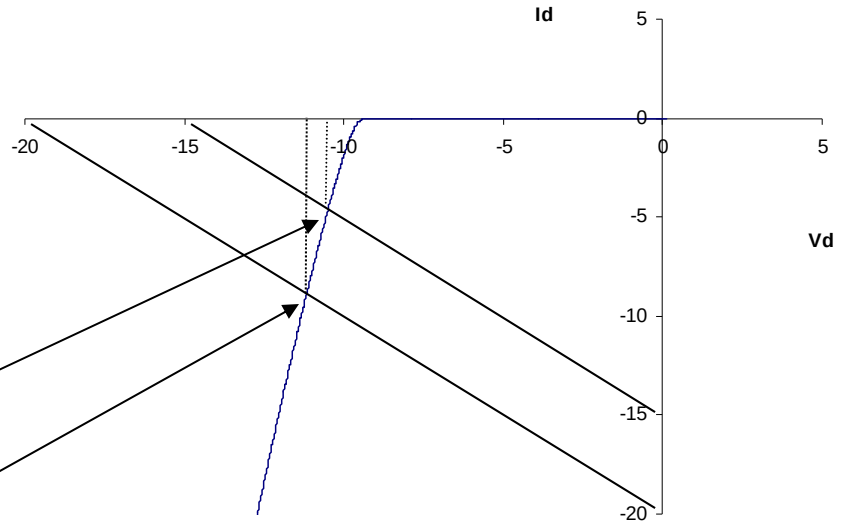
- Load: Change in Output voltage due changes in Load

$$\text{Load Regulation} = \frac{V_{no-load} - V_{full-load}}{V_{full-load}} \times 100\%$$

Zener Diode Regulator

- Load Line: $V_{SS} = -Ri_D - v_D$



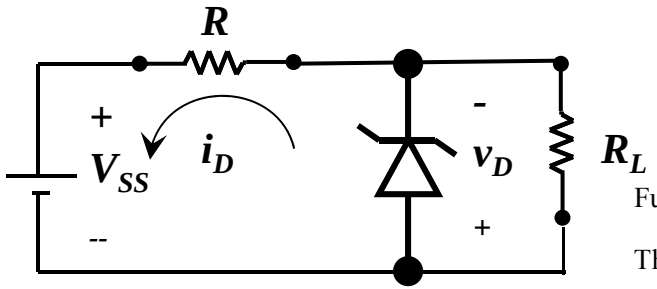


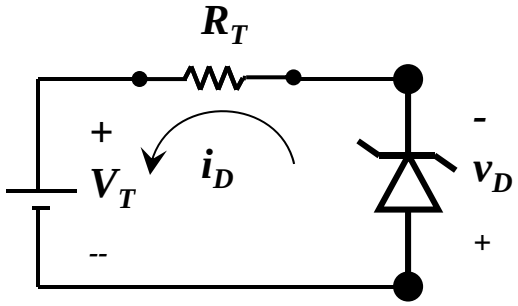
- R=1k, V_{SS}=15
  - v_D = -10.5
- V_{SS}=20
  - v_D = -11

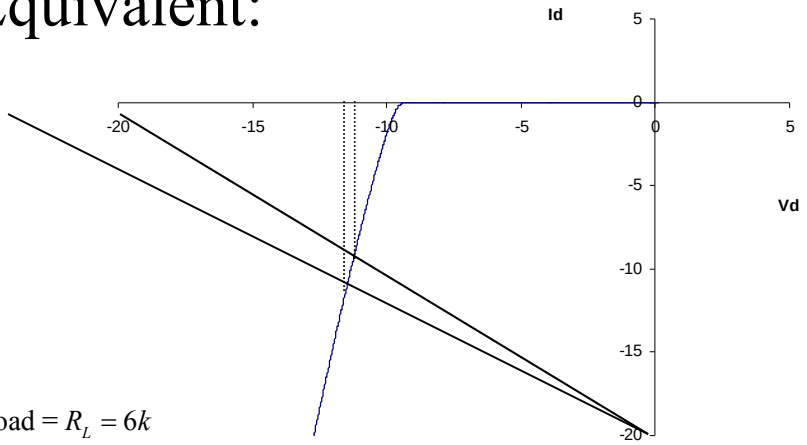
$$\text{Source Regulation} = \frac{\Delta V_{load}}{\Delta V_{SS}} \times 100\% = \frac{.5}{5} \times 100\% = 10\%$$

Zener Diode Regulator

- Load Line Using a Thevenin's Equivalent:
  $V_T = -R_T i_D - v_D$
- $V_{ss} = 24$, $R = 1.2$ k, $R_L = 6$ k







Full Load: Load = $R_L = 6k$

Thevenin's Equivalent: $V_T = \frac{R_L}{R_L + R} V_{SS} = \frac{6}{6+1.2} 24 = 20$

$R_T = \frac{R_L R}{R_L + R} = \frac{6 \times 1.2k}{6+1.2} = 1k$

Load Line Intercepts $v_D = -V_T = -20; i_D = -\frac{V_T}{R_T} = -\frac{20}{1k} = -20m$

$v_D = -11V$

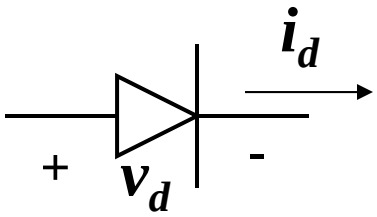
No Load: Load = $R_L = \infty$

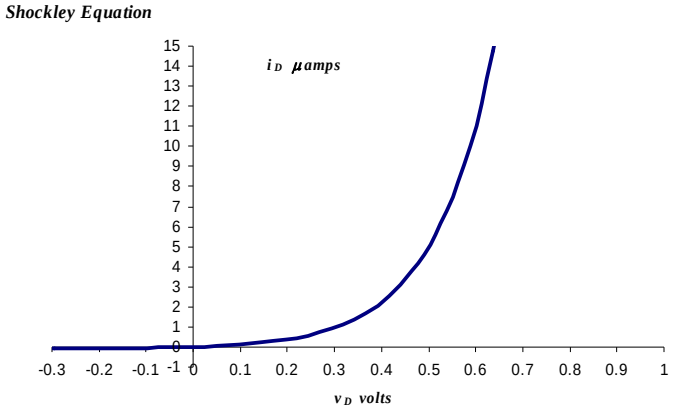
Load Line Intercepts $v_D = -V_{SS} = -24; i_D = -\frac{V_{SS}}{R} = -\frac{24}{1.2k} = -20m$

Load: $v_D = -11.5V$

Load Regulation: $\frac{.5}{11} \times 100\% = 4.5\%$

PN Junctions - Shockley Equation





$i_D = I_S(e^{\frac{v_D}{nV_T}} - 1)$ where i_D and v_D are the diode current and voltage,

I_S is called the reverse bias saturation current,

and V_T is the called the thermal voltage and is

$V_T = \frac{kT}{q}$ where k is the boltzman constant, 1.38×10^{-23} Joule/$^\circ$Kelvin,

T is the temperature of the junction in degrees Kelvin,

and q is the magnitude of electric charge of an electron, 1.60×10^{-19} coulombs

n is called the emission coeficient as takes values between 1 and 2

Small Signal Equivalent Circuit for a Diode Using the Shockley Equation

- We can represent a diode by a resistor if the current and voltage are small signals

Define a resistance near the Q - point :

$$\Delta i_D \cong \left(\frac{di_D}{dv_D}\right)_Q \Delta v_D$$

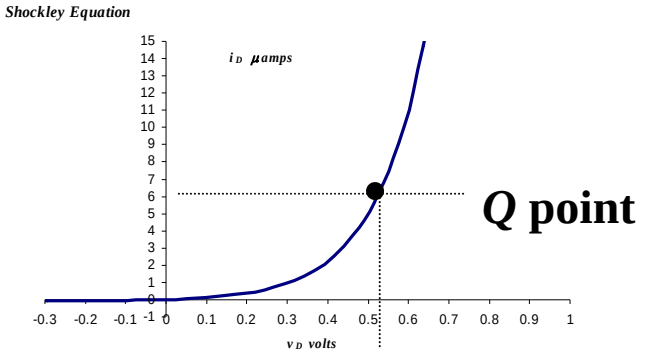
$$r_d = \left[\left(\frac{di_D}{dv_D}\right)_Q\right]^{-1}$$

$$v_d = i_d r_d$$

$$r_d = \left[\left(\frac{d}{dv_D}[I_S(e^{\frac{v_D}{nV_T}} - 1)]\right)_Q\right]^{-1} = \left[\left(I_S \frac{1}{nV_T} e^{\frac{v_{DQ}}{nV_T}}\right)_Q\right]^{-1}$$

$$= \left[I_S \frac{1}{nV_T} e^{\frac{V_{DQ}}{nV_T}}\right]^{-1}$$

where V_{DQ} is the value of v_D at the Q - point



Note that I_{DQ} is the value of i_D

at the Q - point $\cong I_S e^{\frac{V_{DQ}}{nV_T}}$

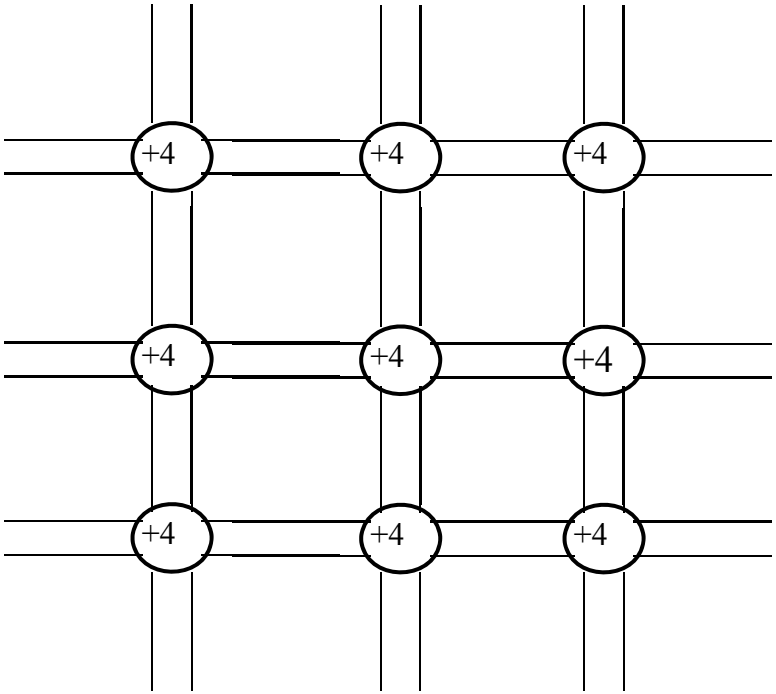
$$r_d = \left[\frac{I_{DQ}}{nV_T}\right]^{-1} = \frac{nV_T}{I_{DQ}}$$

Basic Semiconductor Electronics

- Atomic Structure of Valence-4 elements like Carbon, Silicon, Germanium, etc.
  - have 4 valence electrons in its outer atomic shell
  - these atoms form covalent bonds with 4 other atoms in a lattice
- When the energy levels of these electrons are raised several of these bonds may become randomly broken and a free electron is created
  - as a result these electrons are free to move about in the material similar to electron conduction occurs in a metal
  - in addition to the free electron, a negative particle, a “hole” which is a positive “particle” is created which also moves freely within the material.
- As electrons and holes move through the material, they may encounter each other and recombine and, thereby, become electrically neutral
- This type of material is called an intrinsic semiconductor

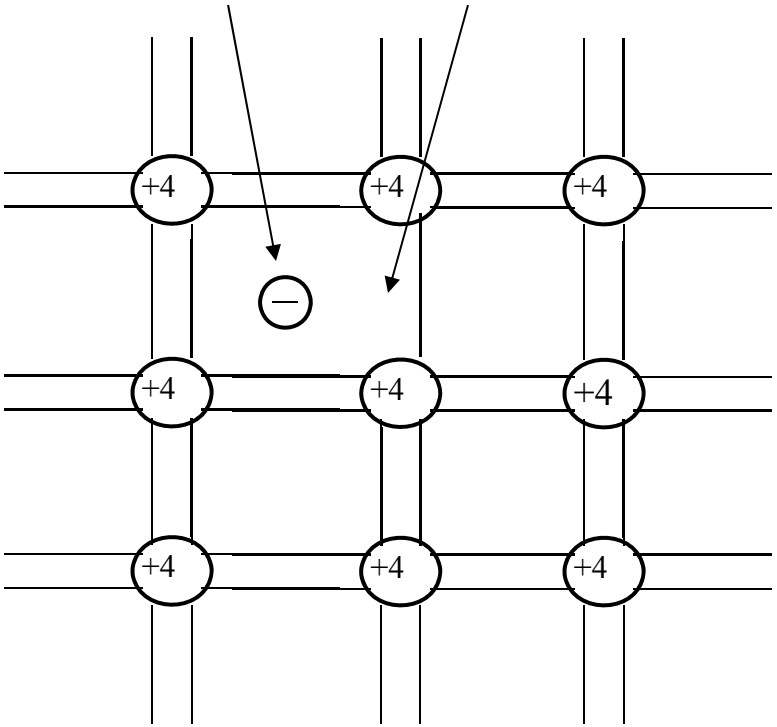
Intrinsic Silicon Crystal

Complete Lattice



Intrinsic Silicon Crystal

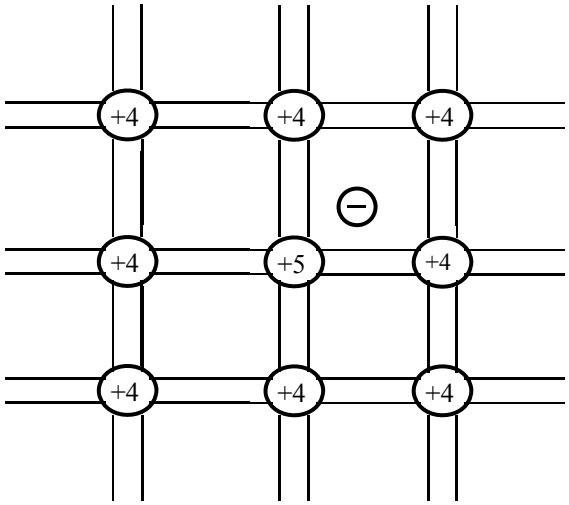
Thermal Energy causes a bond to be broken and a free electron and hole are created

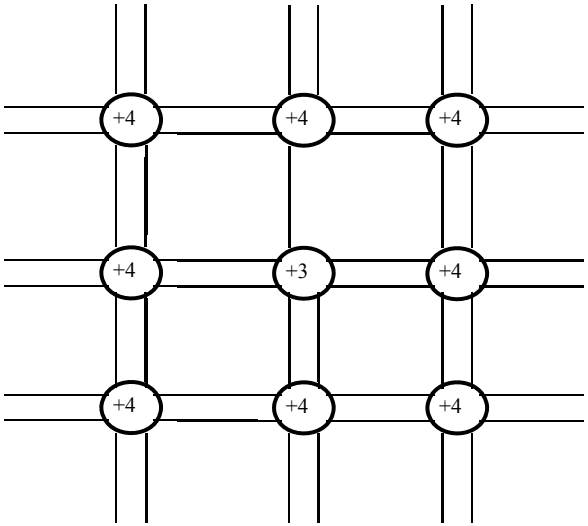


Doped Semiconductor Material

- If we incorporate a small impurity of five or three valence band materials into a 4 valence band lattice, we have created an extrinsic semiconductor which is doped with an impurity
- n-type semiconductor
  - Doping with five valence material (e.g. Arsenic) to create additional free (donor) electrons and a static positive charged ion in the core lattice
  - Majority carriers are electrons; minority carriers are holes
  - The concentration of electrons in a n-type semiconductor = concentration of the donor electrons + the concentration of free holes (which is the same as the number of electrons which have randomly broken their valence bonds)
- p-type semiconductor
  - Doping with three valence material (e.g., Gallium) to create additional free (donor) holes and a static negative charged ion in the core lattice
  - Majority carriers are holes; minority carriers are electrons
  - The concentration of holes in a p-type semiconductor = concentration of the donor holes + the concentration of free electrons (which is the same as the number of holes which have randomly broken their valence bonds)

Doped silicon material





n-type free electrons

p-type free holes

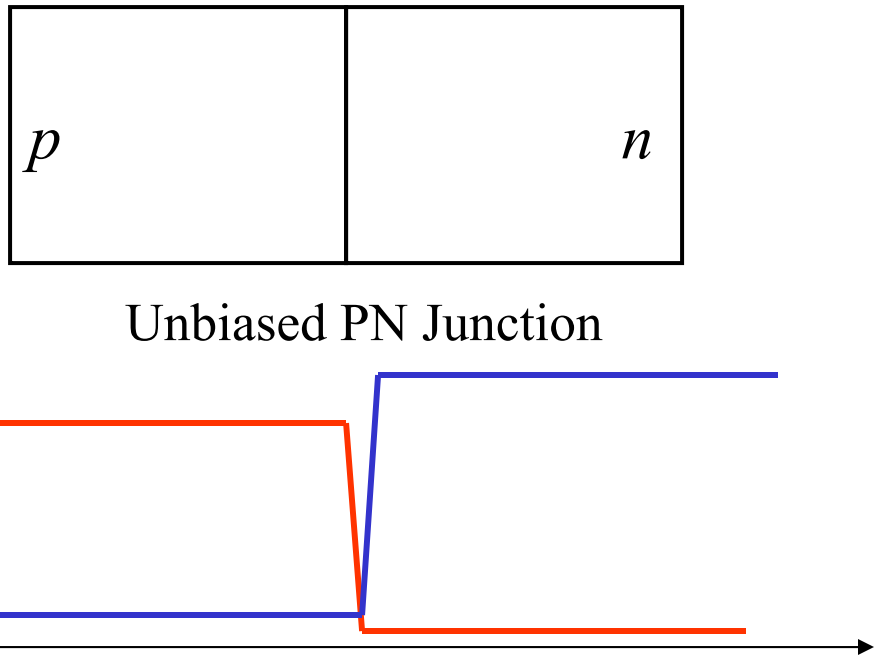
Carrier Concentrations and Recombination

- There are two types of carrier concentrations
  - Majority carriers due to the doping
    - Electrons in n-type
    - Holes in p-type
  - Minor carriers to due thermal excitation
    - Holes in n-type
    - Electrons in p-type
- Recombination: when an electron meets a hole, they combine to complete the bond
- Generation: thermal excitation creates new carriers
- Equilibrium exists when the rate of recombination equals the rate of generation

PN Junction

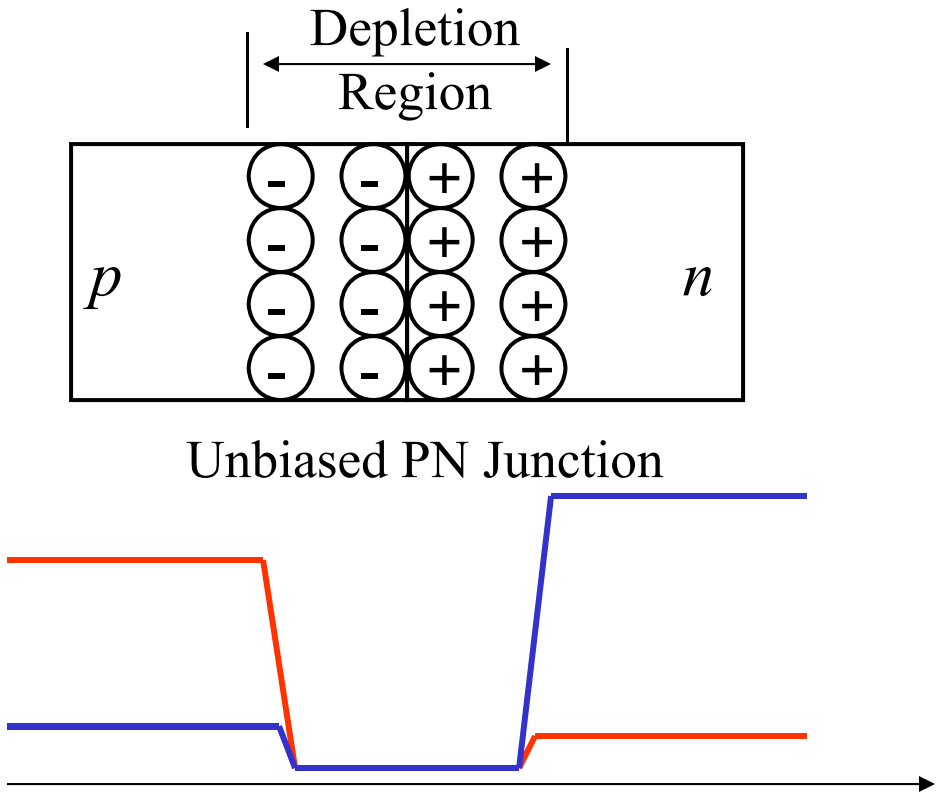
- When a p-type semiconductor is fused with a n-type, the following occurs at the junction.
  - Because the concentration of electrons is greater on n-type side, holes from the p-type diffuse across the junction to the n-type side
  - Likewise electrons diffuse across the junction from the n-type to the p-type material
  - These carriers recombine and what remains are the negatively charged ions on the p-type side and positively charged ion on the n-type side.
- The ions which are tied to the lattice form an electric field which prohibits the flow of carriers across the junction.
  - The area where these ions and their associated electric field are situated is called the depletion region since it is depleted of holes and electrons
  - The electric field which prohibits the flow of carriers is called the barrier potential

PN Junctions Prior to being Fused



Unbiased PN Junction

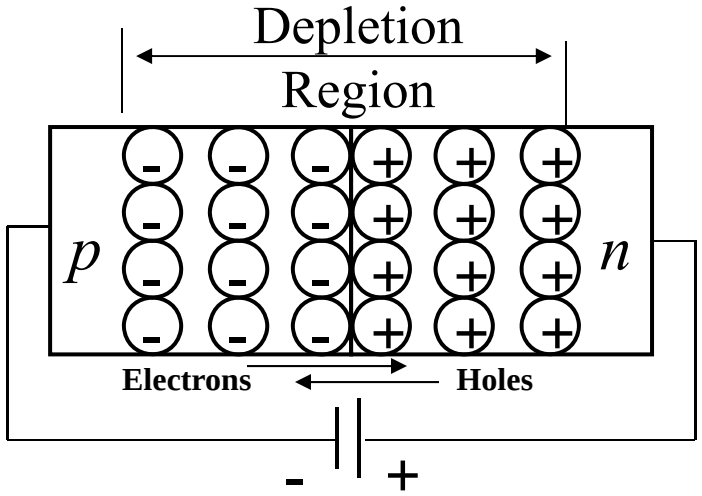
PN Junctions Unbiased



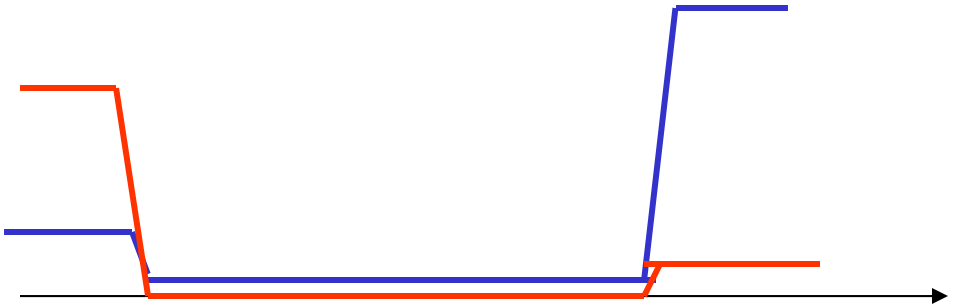
Reverse Bias PN Junction

- When an external voltage is a applied to a PN junction such that the n-type is more positive than the p-type, then we say that the PN junction is reverse-biased and the following happens:
  - The external voltage creates an electric field which enhances the barrier potential and the depletion region becomes wider since the majority carriers are pulled away from the junction (e.g., the electrons in the n-type material are attracted away from the junction by the positive voltage).
  - However, this applied field supports the flow of minority carriers across the junction (e.g., the holes in the n-type material are attracted across the junction by the enhanced electric field of the widened depletion region) and when they cross the junction they become majority carriers (e.g., the minority carrier n-type holes now become majority carriers once they cross the junction to the p-type) and are attracted away from the junction as described above.
  - Since the flow across the junction is due to minority carriers the current flow is small (this is sometimes called the reverse-based leakage current).

PN Junctions Reverse Biased



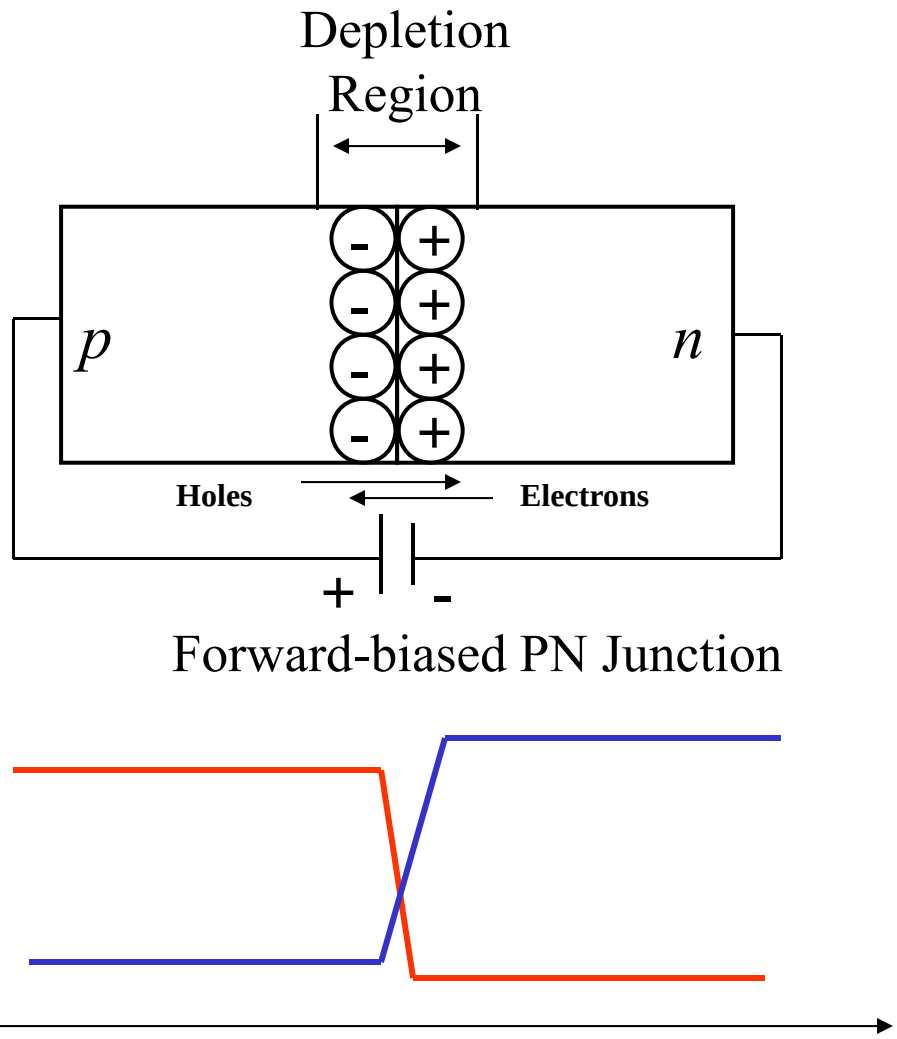
Reverse-biased PN
Junction



Forward Bias PN Junction

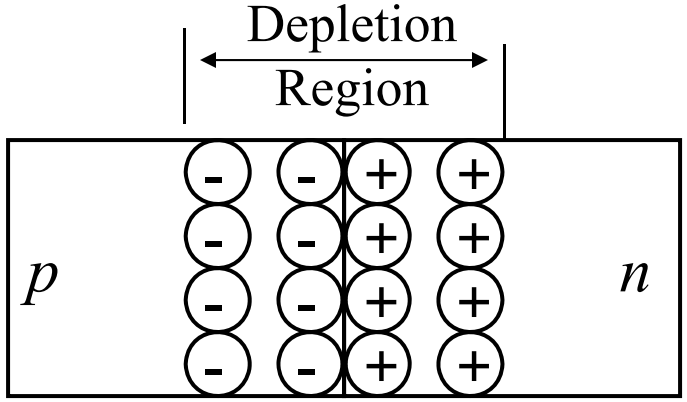
- When an external voltage is a applied to a PN junction such that the n-type is more negative than the p-type, then we say that the PN junction is forward-biased and the following happens:
  - The external voltage creates an electric field which opposes the barrier potential and the depletion region becomes smaller provided it is larger than the voltage barrier of the depletion region (typically, a few tenths of a volt)
  - This allows for the further flow of majority carriers across the junction
  - As the majority carriers cross the junction, the become minority carriers and then recombine the majority carriers on the other side
  - Since the flow across the junction is due to majority carriers the current flow is large.

PN Junctions Forward Biased



Forward-biased PN Junction

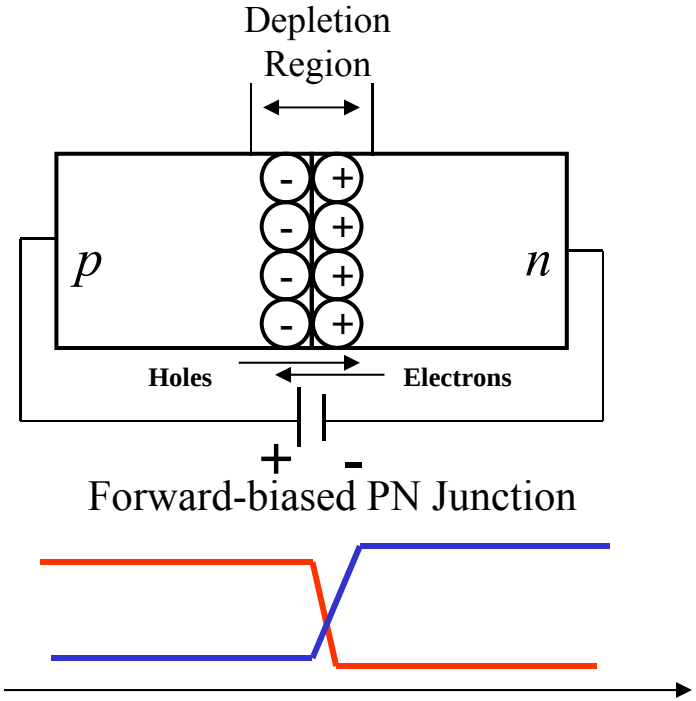
PN Junctions Junction Capacitance



Unbiased PN Junction

- The ions at the junction look like charges on a two plates of a capacitor and, thereby, create a capacitance effect
- We call this the junction capacitance

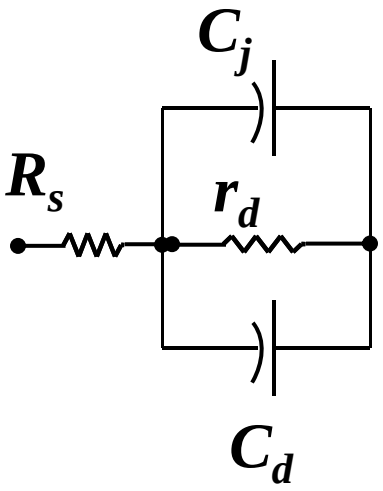
PN Junctions Diffusion Capacitance



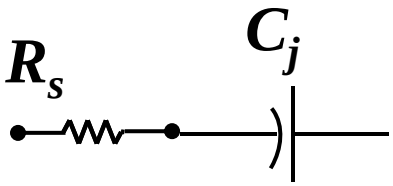
- The charges which cross the junction holes on the *n*-side and electrons on the *p*-side also looks like charges on a two plates of a capacitor and, thereby, adds to the capacitance effect
- We call this the diffusion capacitance

Small Signal Equivalent Circuit Updated

- In addition to the resistance of the junction rd, we need to add the junction capacitance and the diffusion capacitance
- In addition, there is a resistive voltage drop due to bulk of the material on both sides of the junction, Rs
- Now the small signal equivalent circuit becomes:



Forward Biased



Reverse Biased

Homework

- Probs. 3.2, 3.3, 3.5, 3.15, 3.16, 3.17, 3.20, 3.22, 3.24, 3.54, 3.61, 3.62, 3.63, 3.65, 3.73, 3.74
- For problem 3.16a repeat with D2 reversed
- For problem 3.16c repeat with the $+15V$ source replaced by $-15V$