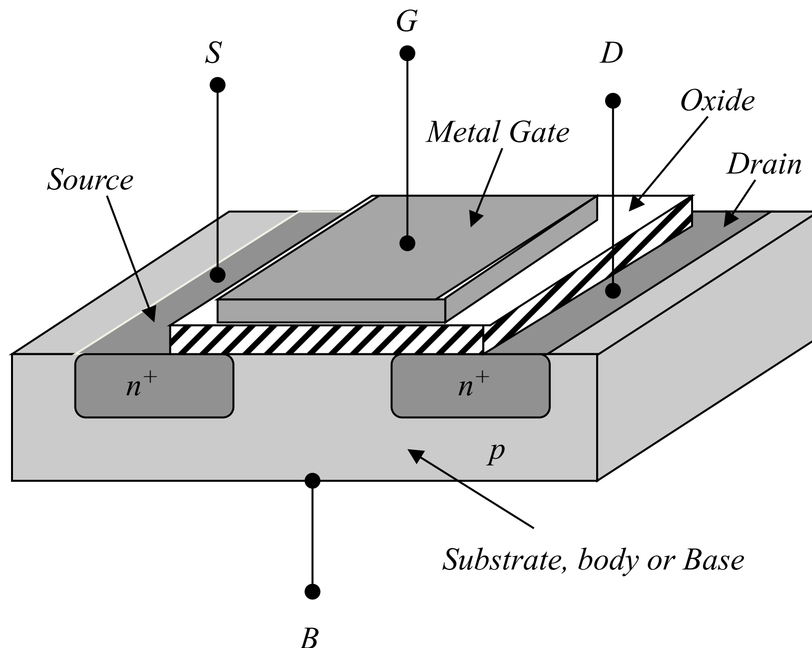
Field Effect Transistors

Lecture 9

Types of FET

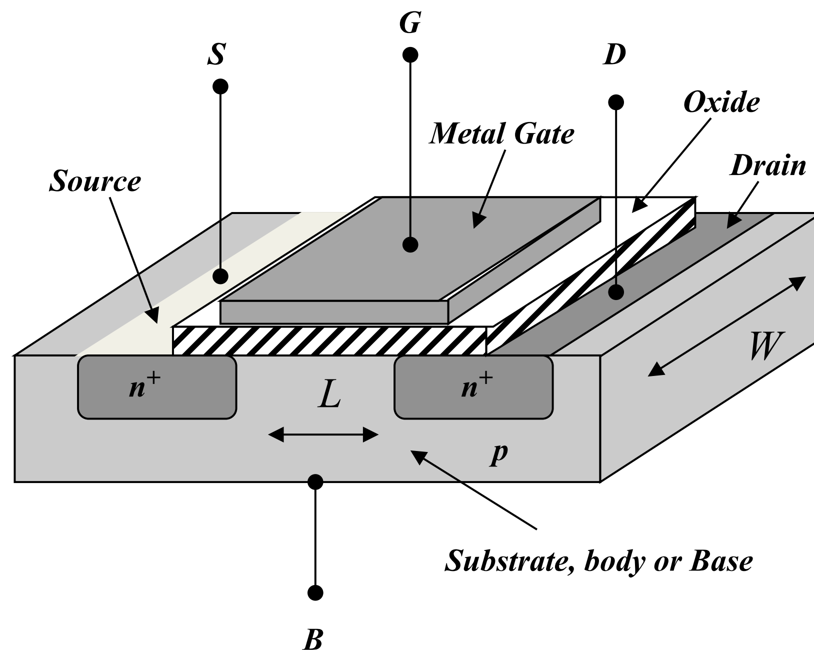
- Metal Oxide Semiconductor Field Effect Transistor – MOSFET
  – Enhancement mode
  – Depletion mode
- Junction FETs
- *p* channel vs *n* channel

Metal Oxide Semiconductor Field Effect Transistor MOSFET (NMOS) Enhancement Mode



- Consists of Four terminals
  - Drain which is *n*-doped material
  - Source also *n*-doped material
  - Base which is *p*-doped material
  - Gate is a metal and is insulated from the Drain, Source and Base by a thin layer of silicon dioxide ~ .05-.1mm thick
- Basically, an electric current flowing from drain to source, i_D, is controlled by the amount of voltage (electric field) appearing between the gate and base (note that the base and source are usually tied together and therefore, it is referred to as the gate to source voltage or gate voltage), v_{GS}.
- i_D flows through a channel of n-type material which is induced by v_{GS}. The amount of i_D is a function of the thickness of the channel and the voltage between drain and source, v_{DS}
- However, the thickness of channel is controlled by the level of gate voltage. (The width, .5 to 500 mm, and length, .2 to 10 mm, of the channel is shown in the diagram.)

Metal Oxide Semiconductor Field Effect Transistor MOSFET (NMOS) Enhancement Mode



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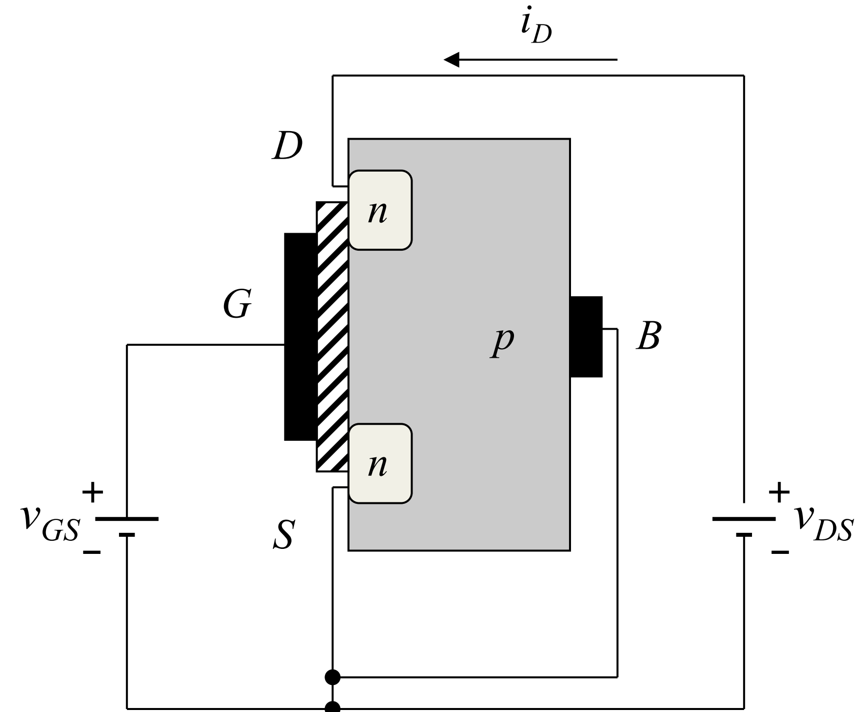
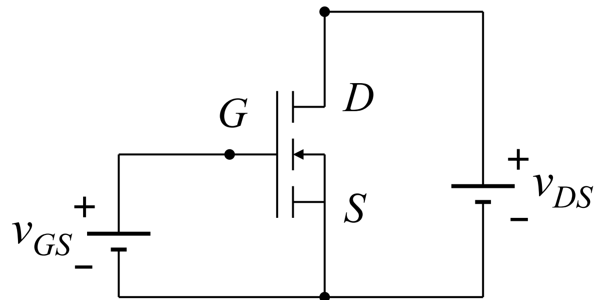
Modes of the NMOS
Cutoff

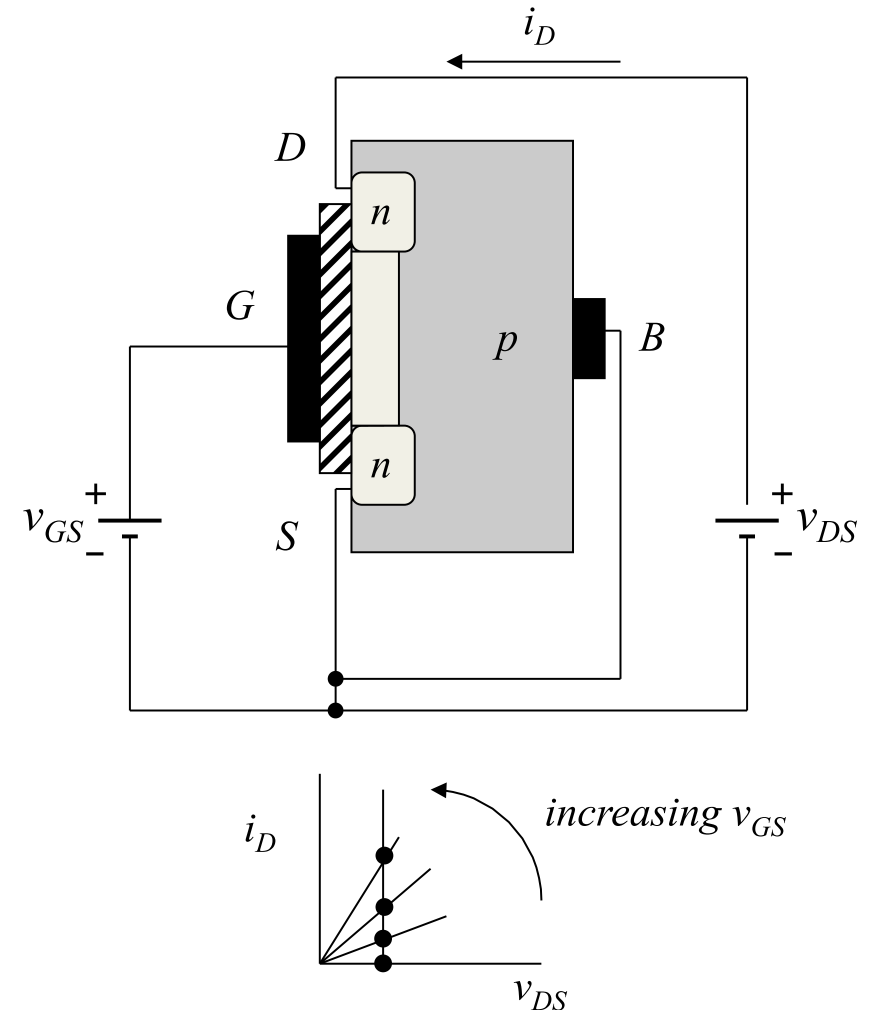
- $v_{GS} = 0$
- *pn* junctions at the drain and source are reverse biased due to v_{DS}
- i_D is zero





Modes of the NMOS
Triode Region

- $v_{GS} \geq V_{to}$ a threshold voltage which causes electrons in the base to be attracted to and holes to be repelled from the region just below the gate
- This process causes a n-type channel to form below the gate
- As v_{DS} is increased, i_D starts to flow. For small values of v_{DS}, i_D is proportional to v_{DS}
- In addition, i_D is proportional to v_{GS}-V_{to}, the excess gate voltage
- Therefore, the MOSFET can act as a voltage controlled resistor in the Triode Region (e.g., used in AGC circuits)



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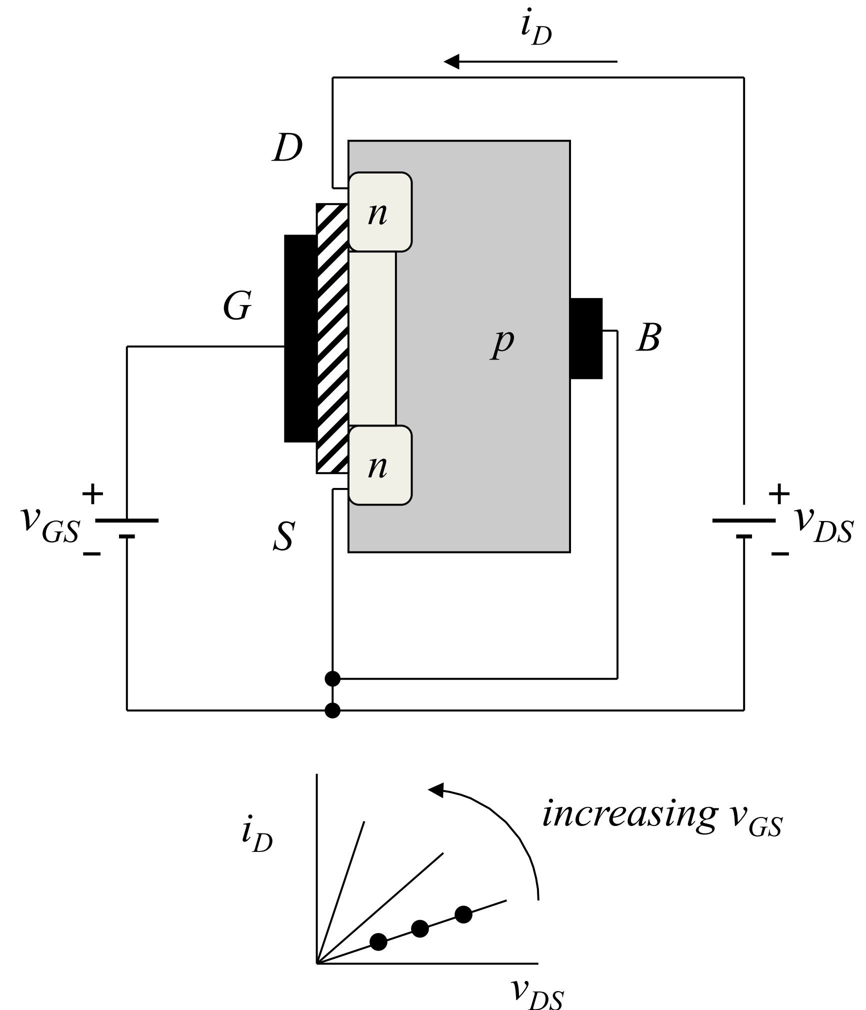


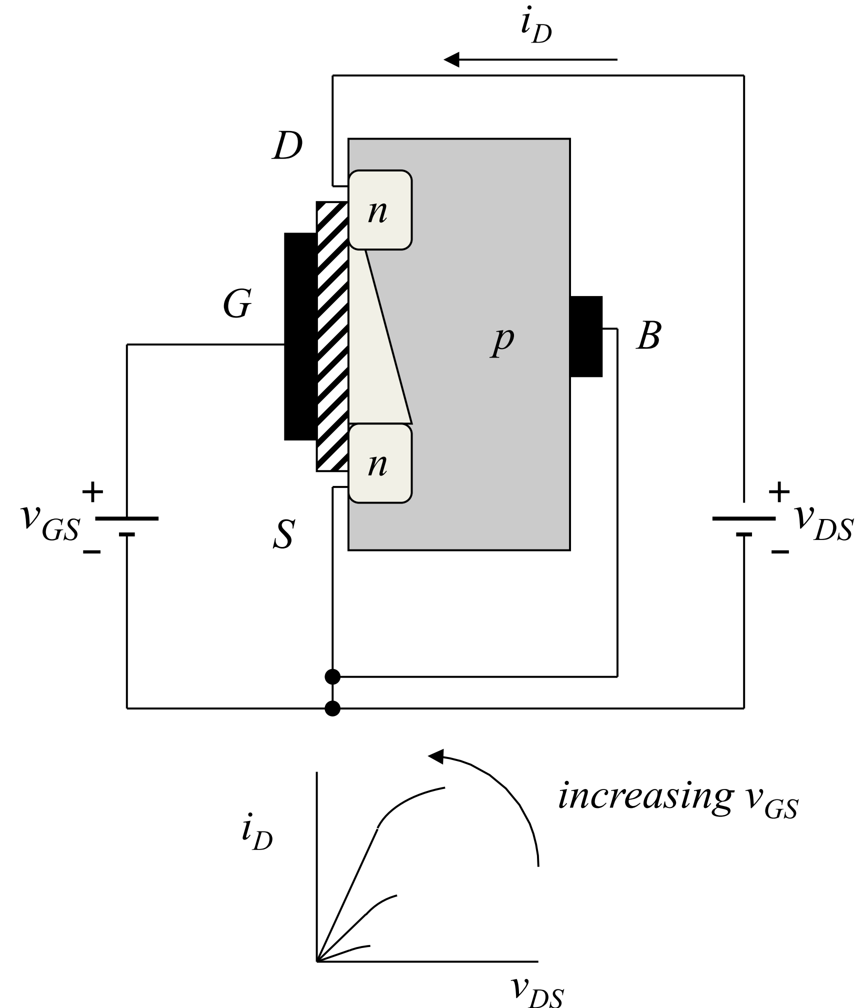
Modes of the NMOS Triode Region (Continued)

- Since the drain is more positive than the source, the voltage difference between the channel and the gate varies along the channel from drain to source.
- As v_{DS} is further increased, this channel voltage profile causes a tapering of the channel thickness. $v_{GD} \neq v_{GS}$
- This tapering causes the resistance of the channel to increase (as v_{DS} increases) and, thereby, reduces the rate of increase of i_D.
- Furthermore, it can be shown that

$$i_D = K[2(v_{GS} - V_{to})v_{DS} - v_{DS}^2]$$

$$K = (\frac{W}{L})(\frac{KP}{2}) = (\frac{W}{L})(\frac{\mu_n C_{ox}}{2})$$

- To summarize: $v_{GS} \geq V_{to}$ and $v_{DS} < v_{GS} - V_{to}$

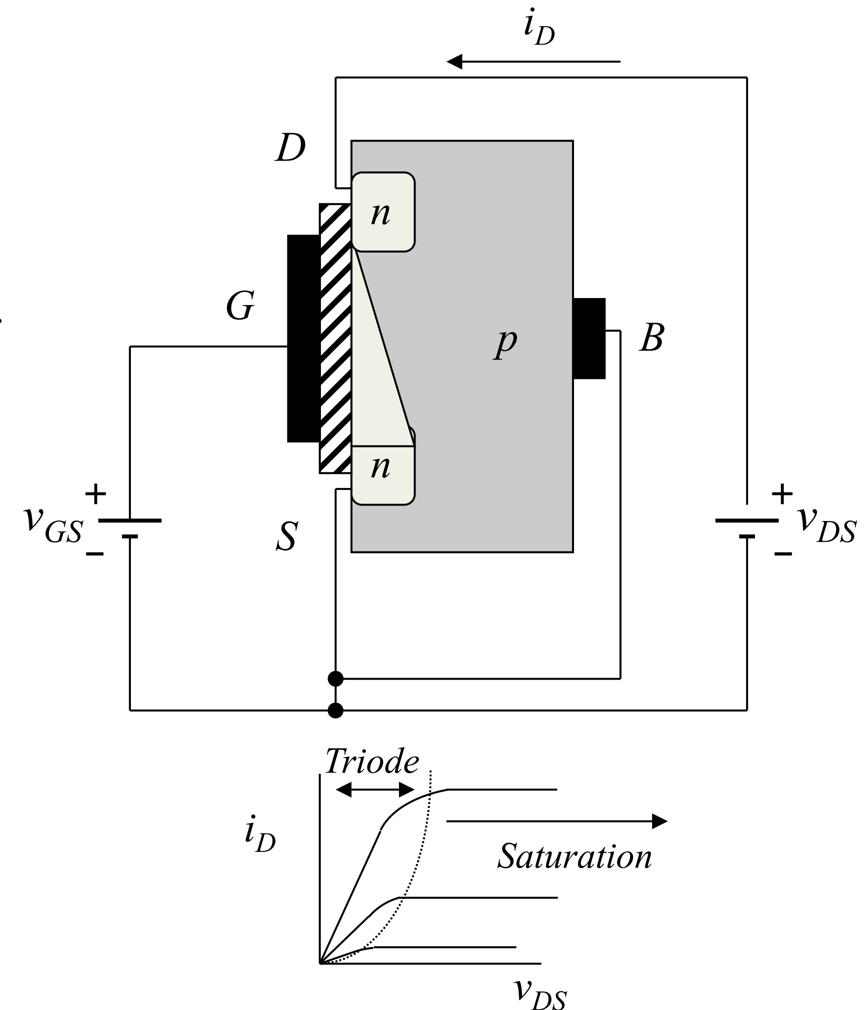


Modes of the NMOS Saturation

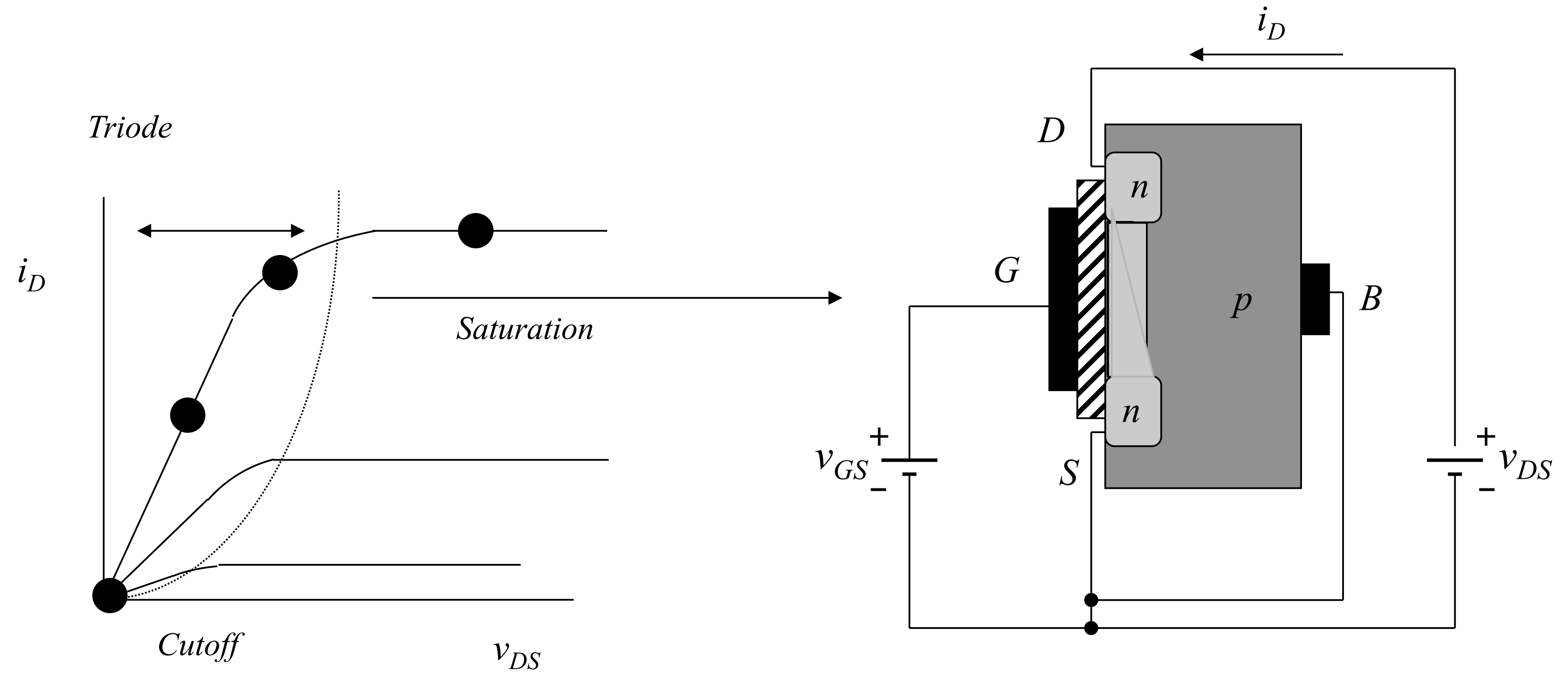
- As v_{DS} continues to increase, the voltage profile continues to taper. When the gate to channel voltage at the drain, v_{GD}, approaches V_{to}, the thickness of the channel at the drain is (virtually) zero. (Note that although the channel thickness is virtually zero, current flow is not cutoff since it is needed to support the channel voltage profile.)
- This phenomenon limits the amount of drain current (i.e., i_D is saturated) and causes i_D to be independent of v_{DS}
- Furthermore, it can be shown that

$$i_D = K(v_{GS} - V_{to})^2$$

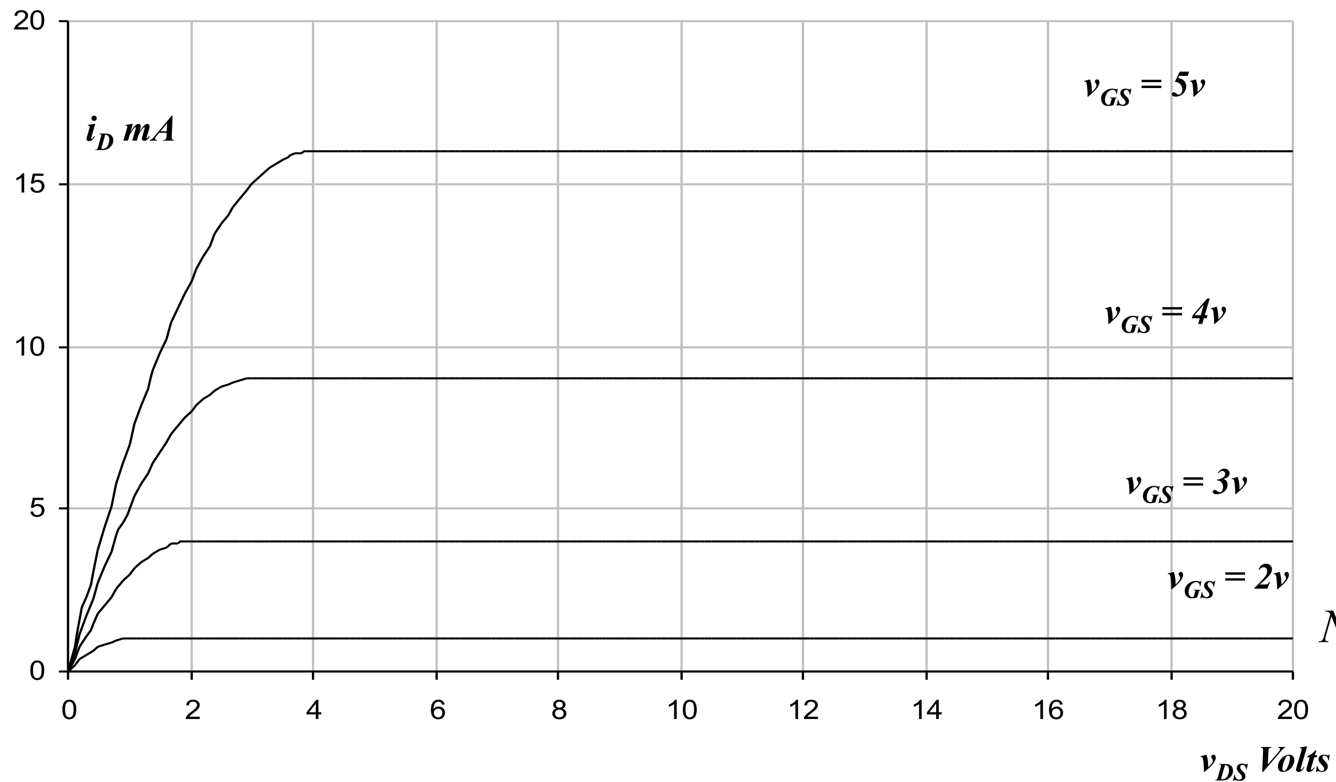
- Summarize: $v_{GS} \geq V_{to}$ and $v_{DS} \geq v_{GS} - V_{to}$



Modes of the NMOS



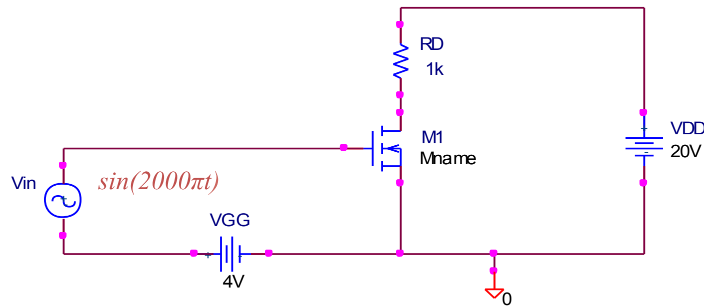
NMOS Characteristics



Note that $V_{to} = 1$

Note that for NMOS devices with short channel lengths, a tilt may exist due to the modulation of the channel length by the depletion region surrounding the drain.

Load Line of a NMOS Amplifier

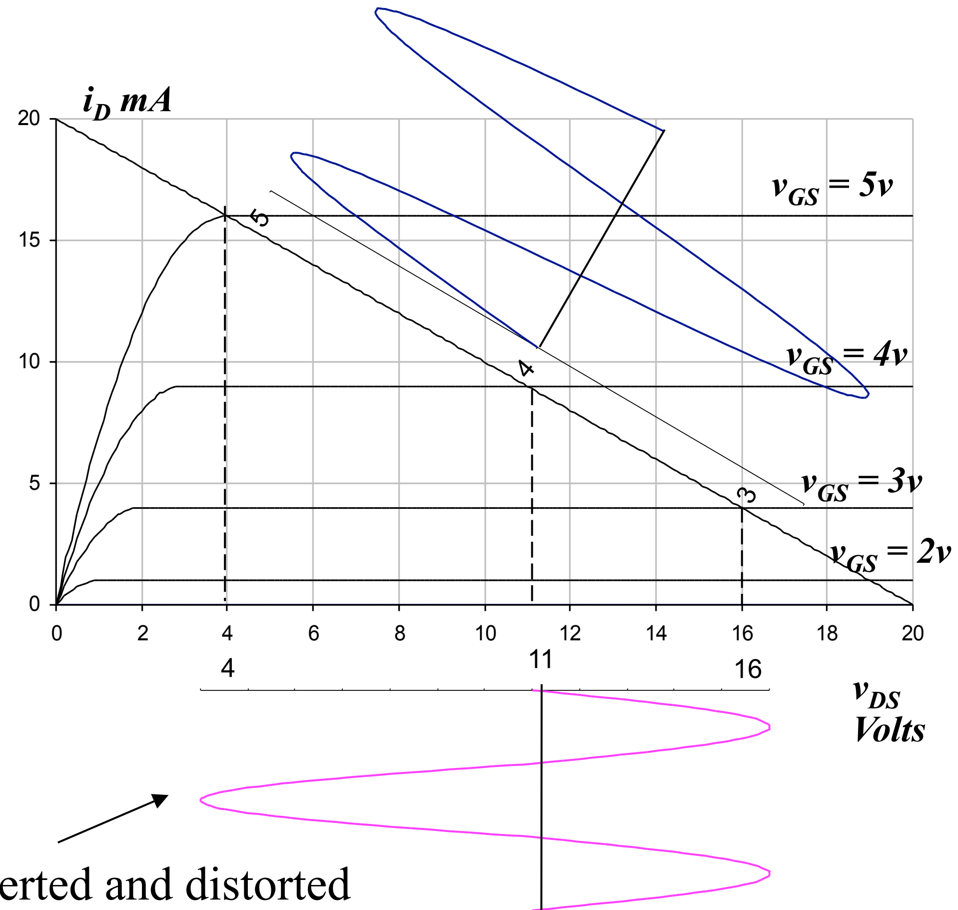


Gate Circuit

$$v_{GS} = v_{in}(t) + VGG$$
$$= \sin(2000\pi t) + 4$$

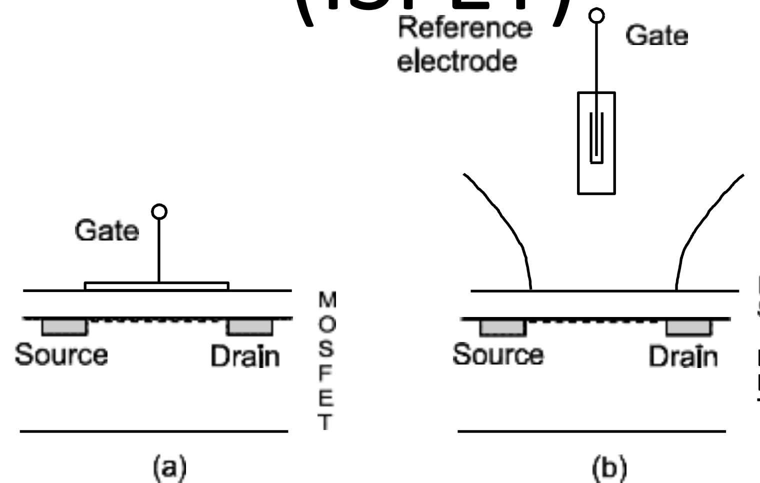
Drain Circuit

$$VDD = i_D RD + v_{DS}$$
$$20 = i_D 1000 + v_{DS}$$



Inverted and distorted

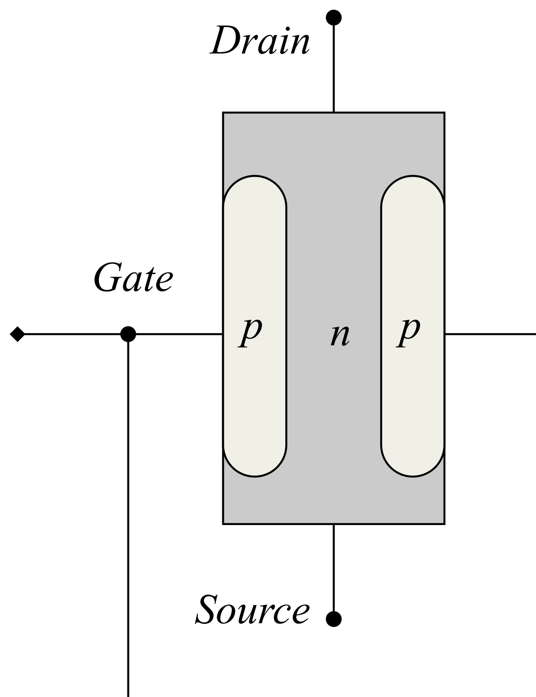
Ion Sensing Field Effect Transistor (ISFET)

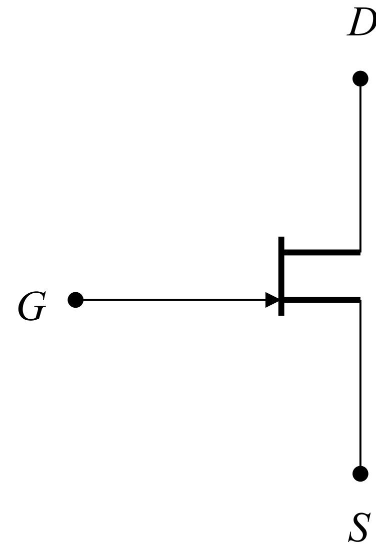


- $\Delta\phi = RT/F \ln (c_1/c_2)$
- R is the gas constant, T the absolute temperature (K) and F the Faraday constant and c_i, are ion concentrations in the solution and oxide.
- Using hydrogen ions can be used to measure pH[1] and DNA[2]

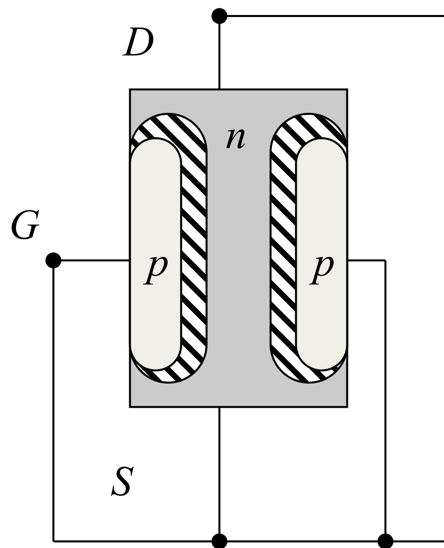
[1] Bergveld, P. **ISFET, Theory and Practice,** IEEE SENSOR CONFERENCE TORONTO, OCTOBER 2003
[2] DNA Electronics, http://dnae.co.uk/technology/overview/

n-channel Junction FET

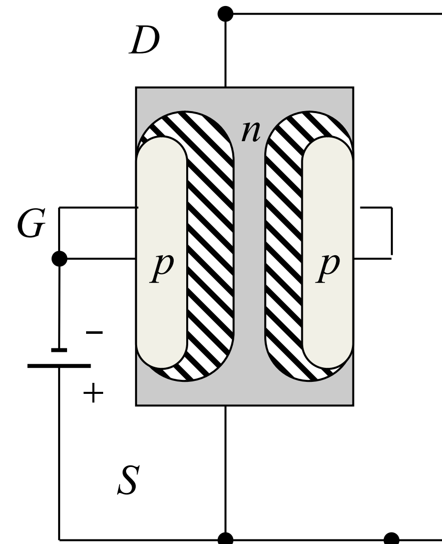




N-channel JFET Gate Bias

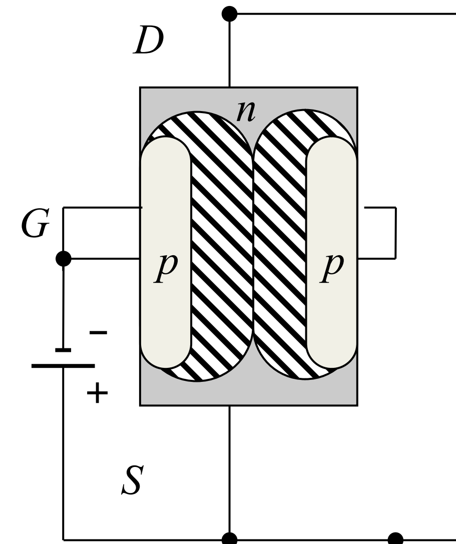


Zero Bias and depletion layer is thin and conduction channel exists from drain to source



$0 > v_{GS} > V_{to}$

Small bias results in larger depletion layer and smaller channel

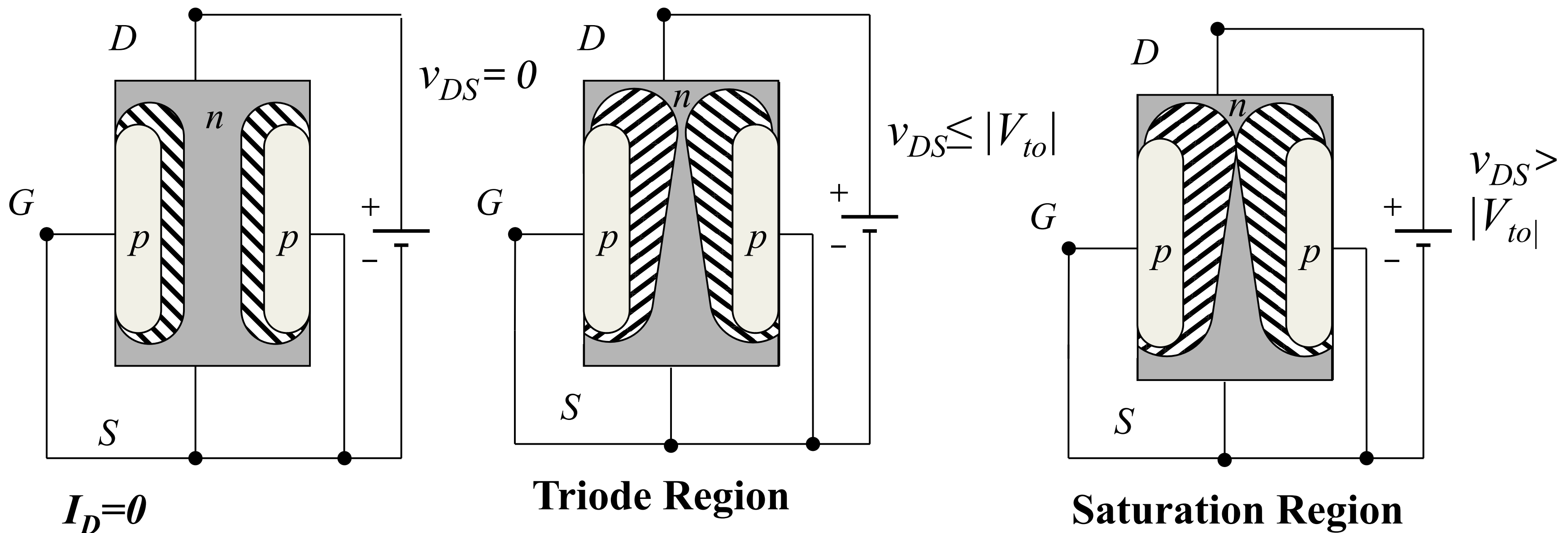


$v_{GS} \leq V_{to}$

Larger bias > pinch-off voltage, V_{to}, creates overlapping depletion layer and no conductive path from drain to source

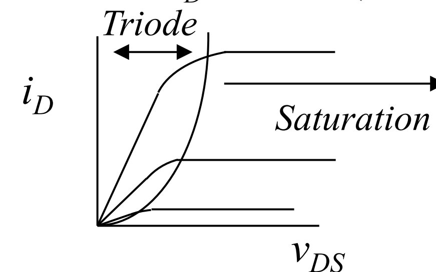
Cutoff Region

n-channel JFET Operation

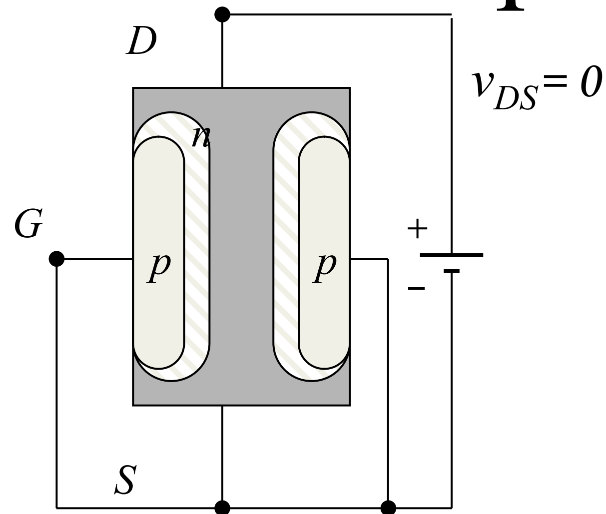


With $v_{GS}=0$, we increase v_{DS} and enter the Triode Region. As a result I_D increases and is proportional to v_{DS}. As v_{DS} increases further, the depletion region between drain and gate grows (with a larger area nearer the drain) and adds more resistance in the channel by narrowing its width. Thus, the rate of drain current increase slows down with increasing v_{DS}. As v_{DS} reaches the pinch-off voltage, V_{t0}, the drain current, I_D saturates (i.e., the FET is in the Saturation Region).

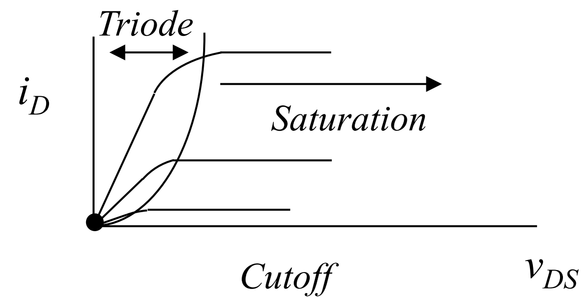
With $v_{GS}<0$, the same phenomenon occurs as v_{DS} is increased. However, the non-zero value of v_{GS} increases the resistance in the channel due to a large depletion layer and therefore, values of I_D are smaller both in the Triode and Saturation regions.



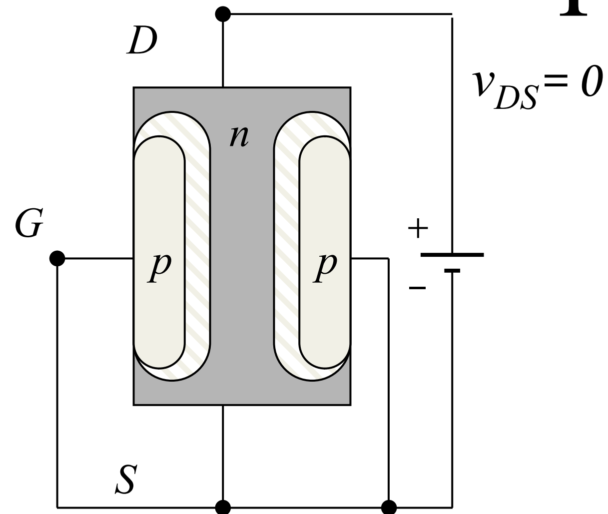
n-channel JFET Operation



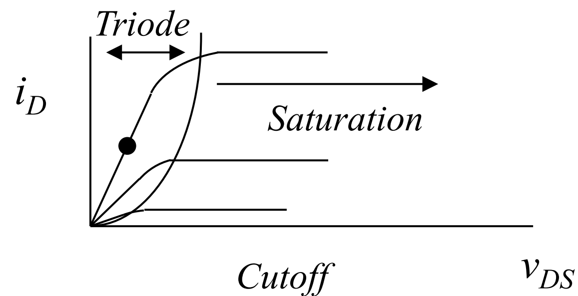
As v_{DS} increase I_D increases and JFET enters the Triode Region.



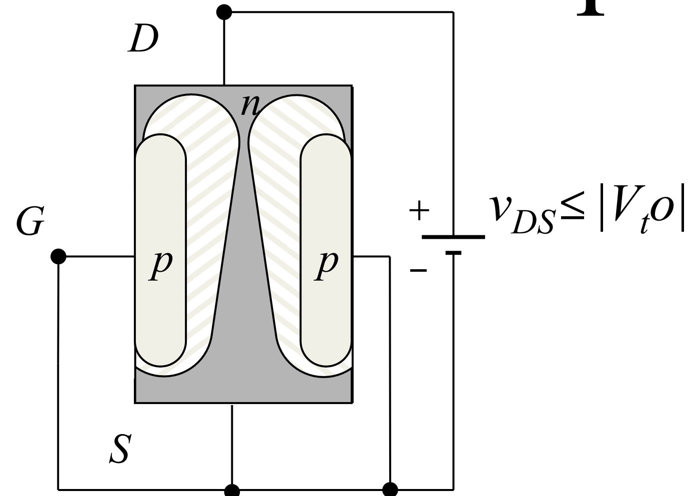
n-channel JFET Operation



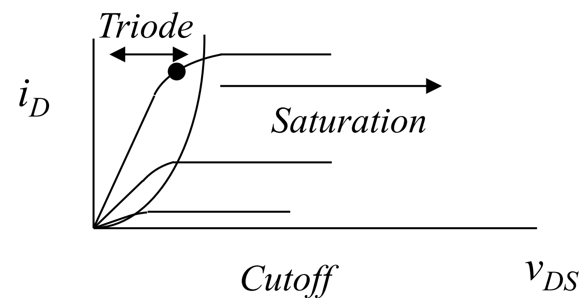
Triode Region
Because the channel is "wide", I_D is proportional to v_{DS}.



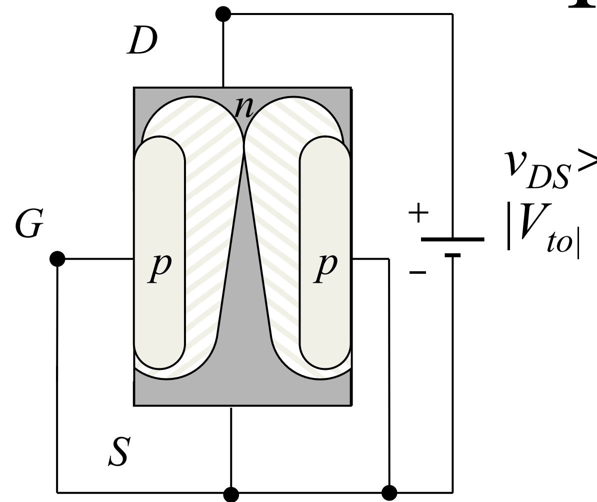
n-channel JFET Operation



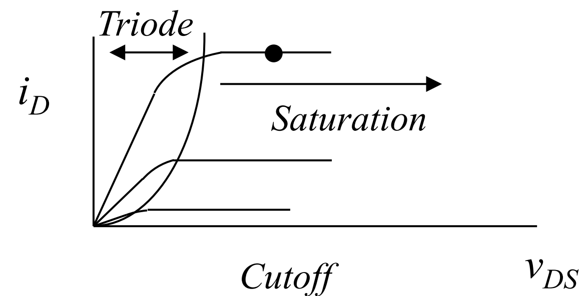
Triode Region
While v_{DS} increases, the depletion region also grows with a larger area at the drain. As a result, the channel resistance increases and increases in I_D are reduced.



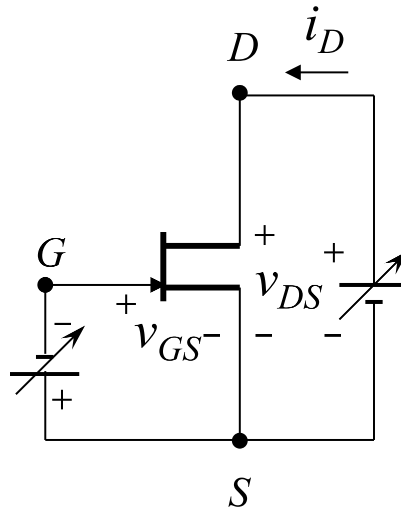
n-channel JFET Operation

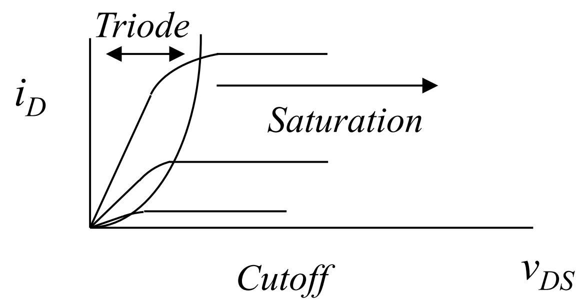


Saturation Region **The depletion region increases as v_{DS} increases. As a result, the depletion region is "pinched off" and I_D does not increase any further (i.e., I_D is saturated).**

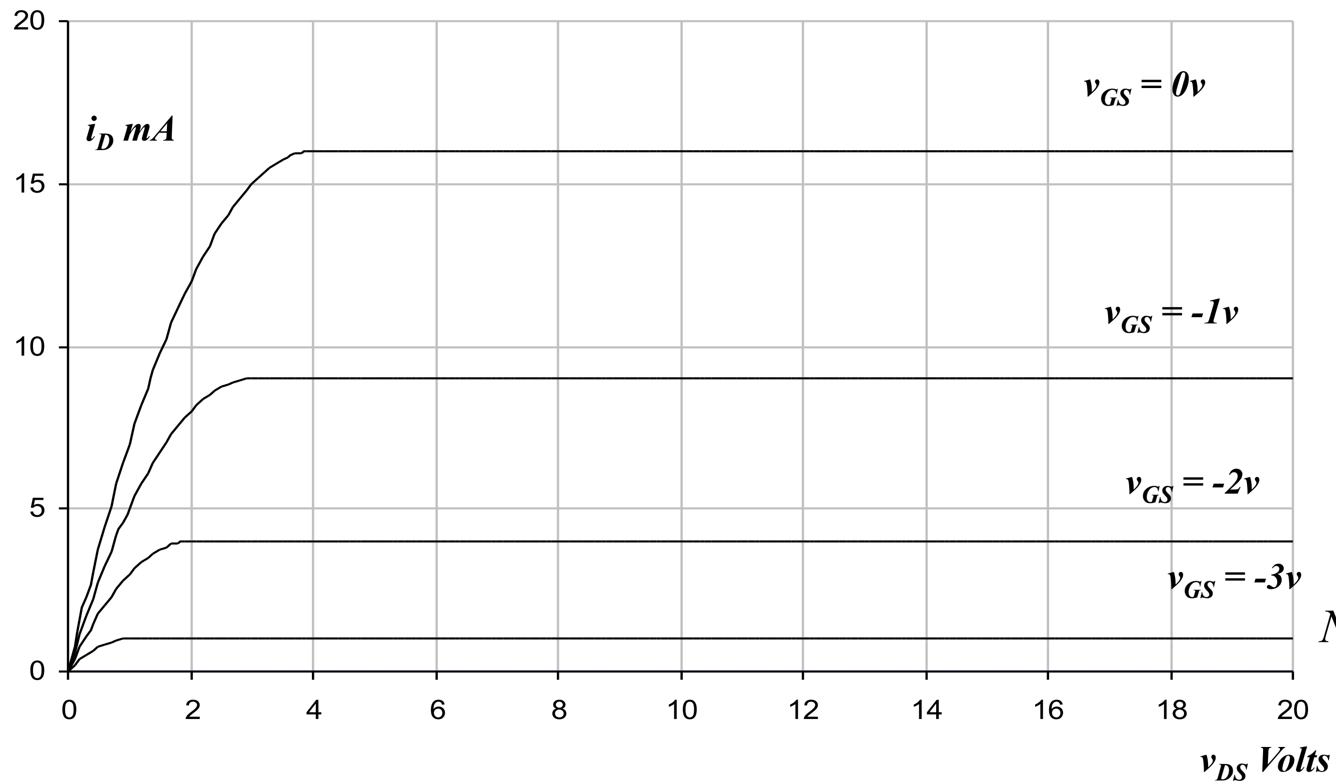


n-channel JFET Operation





JFET Characteristics

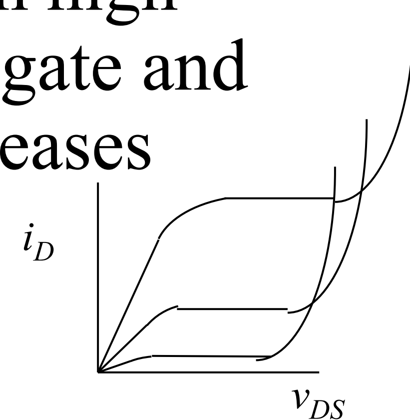


Note that V_{to} = -4

Note that for NMOS devices with short channel lengths, a tilt may exist due to the modulation of the channel length by the depletion region surrounding the drain.

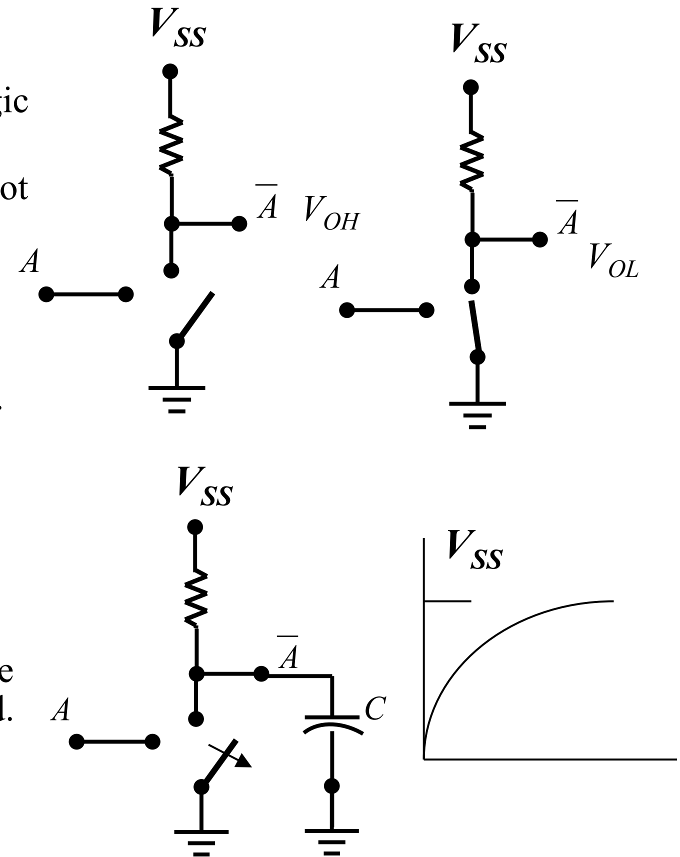
Regions of the JFET

- Cutoff: $v_{GS} < V_{to},\ i_D = 0$
- Triode: $v_{GS} \geq V_{to},\ 0 \leq v_{DS} < v_{GS} - V_{to},\ i_D = K[2(v_{GS} - V_{to})v_{DS} - v_{DS}^2]$
- Saturation: $v_{GS} \geq V_{to}$ and $v_{DS} \geq v_{GS} - V_{to},\ i_D = K(v_{GS} - V_{to})^2$
  - Manufacturer's parameter: Zero-Bias Saturation Current which is the drain current at saturation when $v_{GS} = 0$: $I_{DSS} = KV_{to}^2$
- Breakdown: this region is associated with high values of v_{DS} when the junction between gate and drain breaks down and drain current increases very rapidly.



Device Power Considerations

- Static or Quiescent Power
  - This is power consumed after the device has reached a logic 0 or logic 1.
  - In general, when a device is in a high state, the device is not conducting (i.e., open) and the output is equal to the V_{OH} (i.e., the supply voltage). In this case, no power is consumed.
  - However, when a device is in a low state, the device is conducting (i.e., closed) and the output is equal to the V_{OL}. In this case, there is (static) power being consumed.
  - Therefore, when designed ICs we need to understand the requirements for the power supply and temperature characteristics of the devices.
- Dynamic Power Dissipation
  - Since the fan out load on a gate has a significant capacitive component, a non-zero switching time will be experienced. During this period the device will dissipated power.
  - The power dissipated for a device being switch at a frequency f is given below and is highly dependent on f.



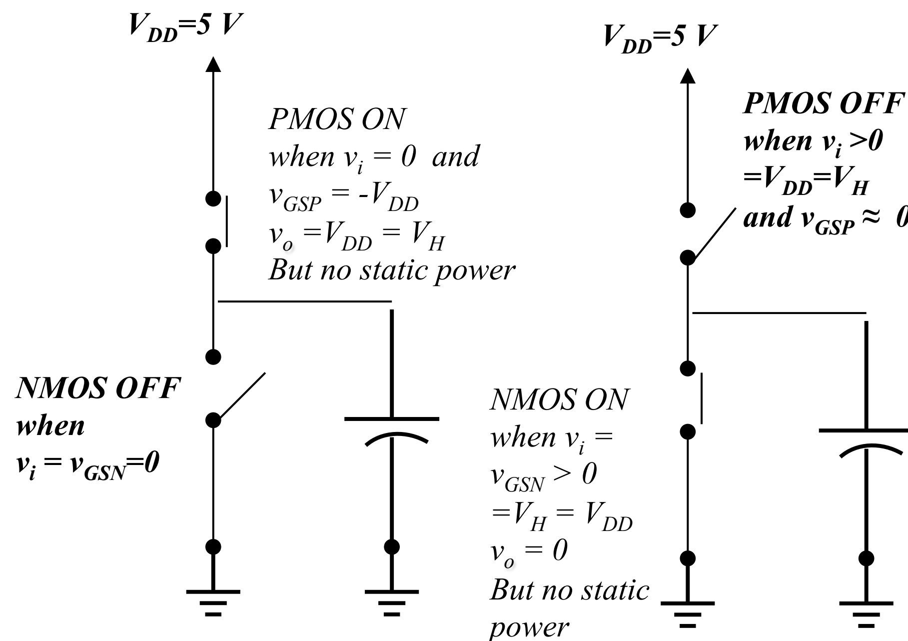
$Q = CV_{SS}$ is the charge on the capacitance when high is reached

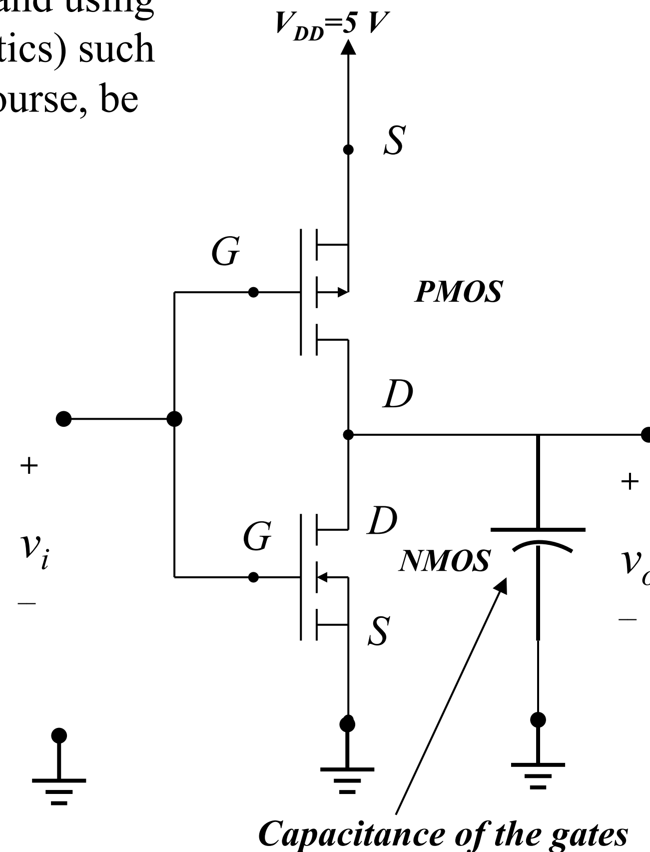
$E = QV_{SS} = CV_{SS}^2$ is the energy needed to achieve the high state as well as released well switching to the low state

$P = fCV_{SS}^2$ is the power dissipated during the switching periods

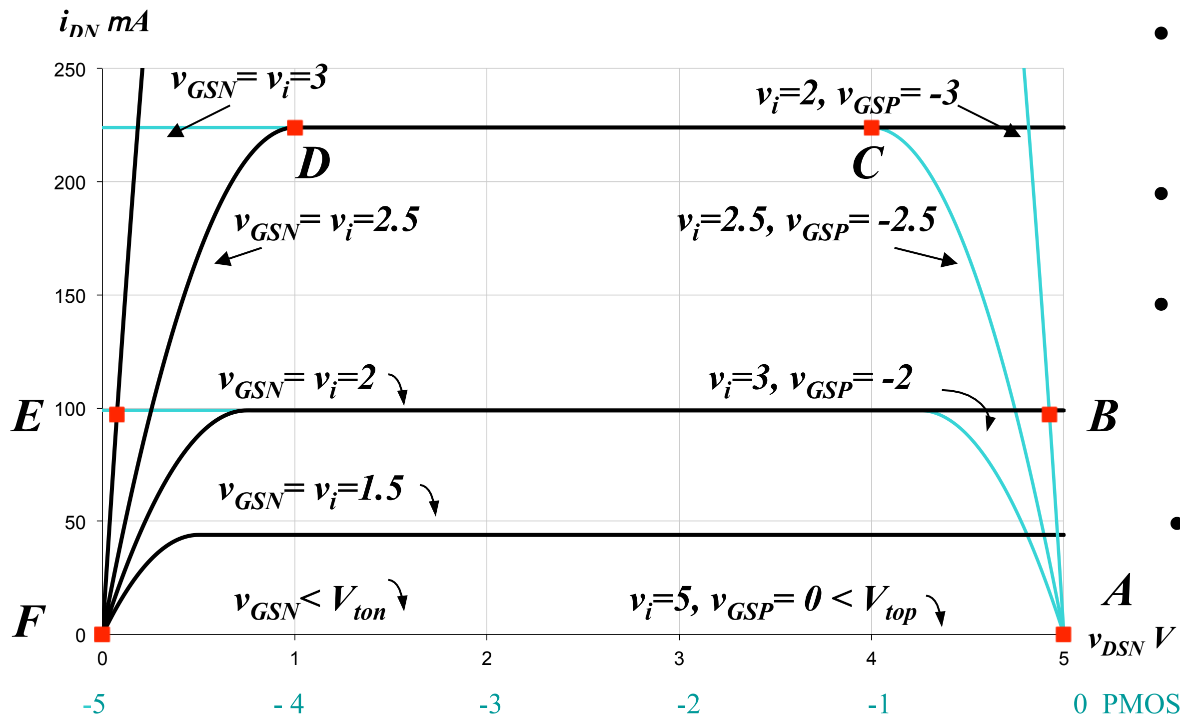
Complementary MOS CMOS

- Taking NMOS (*n*-channel) and PMOS (*p*-channel) and using them in a complementary fashion (same characteristics) such that the static power is always zero (there will, of course, be dynamic power dissipated).
- Note that $V_{GSP} = v_i - V_{DD}$ and $V_{GSN} = v_i$





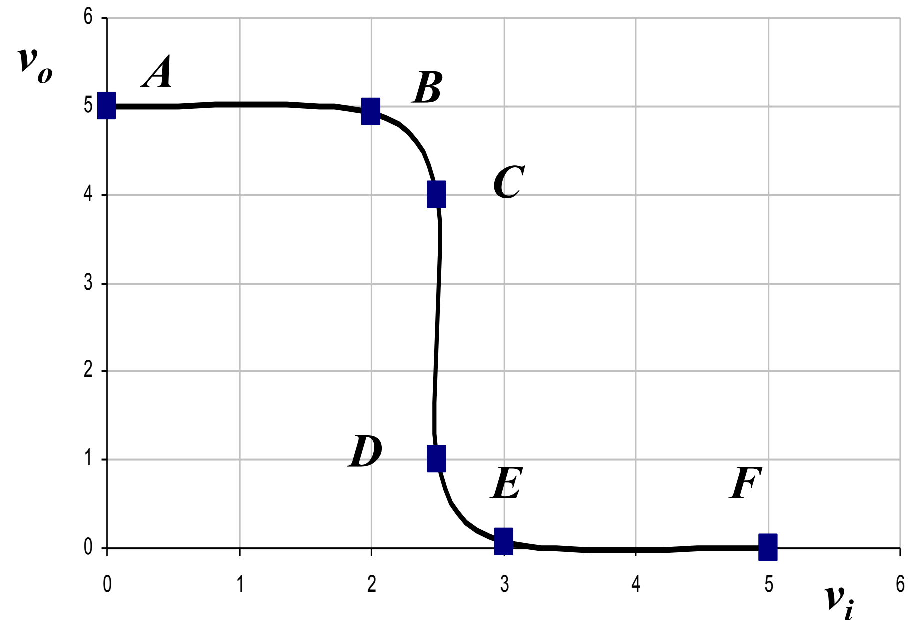
Graphical Analysis



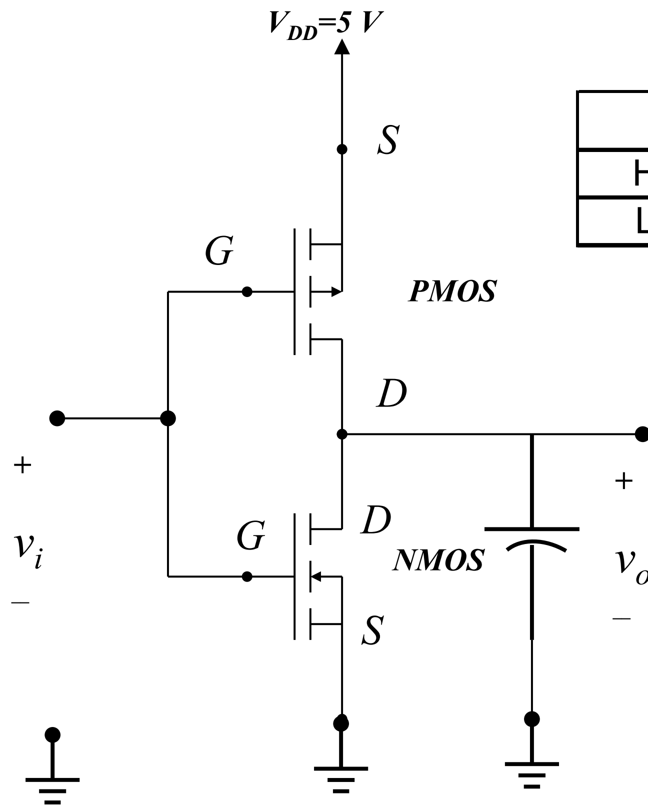
- For CMOS, the load line of the NMOS is the characteristic curves of the PMOS.
- Let view the operation as v_i goes from *0* to *5 V*
- Point A: $v_i=0$, the NMOS is cutoff since $v_i = v_{GSN} < V_{ton}$; the PMOS is conducting since $v_{GSP} = v_i - V_{DD} = -V_{DD}$
- Point B: $v_i=2$ and is the intersection of $v_{GSN} = 2$ and $v_{GSP} = -3$ where the NMOS is in saturation and the PMOS is in the triode region.
- Points C through D: $v_i=2.5$ and is the intersection of $v_{GSN} = 2.5$ and $v_{GSP} = -2.5$ where the NMOS and the PMOS are both in saturation.
- Point E $v_i=3$ and is the intersection of $v_{GSN} = 3$ and $v_{GSP} = -2$ where the NMOS is in the triode region and the PMOS is in the saturation region.
- Point F: $v_i=5$, the NMOS is conducting but the PMOS is cutoff since $v_{GSP} < V_{top} = v_i - V_{DD} = 0$

Transfer Characteristics

- These characteristics approach the ideal characteristics we discuss previously.
- For $v_i < V_{ton}$, $v_o = V_{DD}$
- For $v_i > V_{DD} - |V_{top}|$, $v_o = 0$
- The transfer characteristics fall abruptly at $v_i=V_{DD}/2$



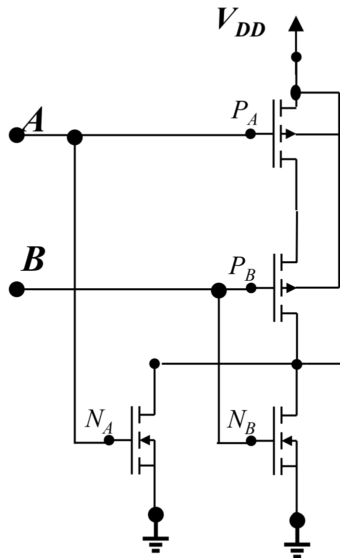
CMOS Inverter Truth Table



v_i		NMOS	PMOS	v_o	
High	1	ON	OFF	Low	0
Low	0	OFF	ON	High	1

CMOS NOR and NAND GATES

NOR Gate

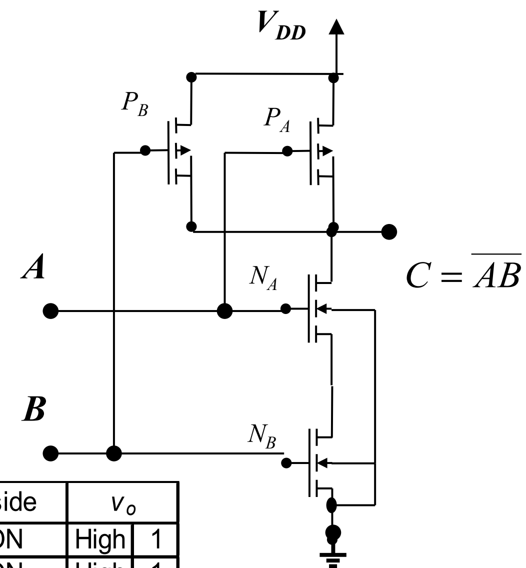


$C = \overline{A + B}$

A		B		NA	PA	NB	PB	Nside	Pside	v_o	
0	Low	0	Low	OFF	ON	OFF	ON	OFF	ON	High	1
0	Low	1	High	OFF	ON	ON	OFF	ON	OFF	Low	0
1	High	0	Low	ON	OFF	OFF	ON	ON	OFF	Low	0
1	High	1	High	ON	OFF	ON	OFF	ON	OFF	Low	0

$$Nside = NA + NB$$

$$Pside = PA \bullet PB$$



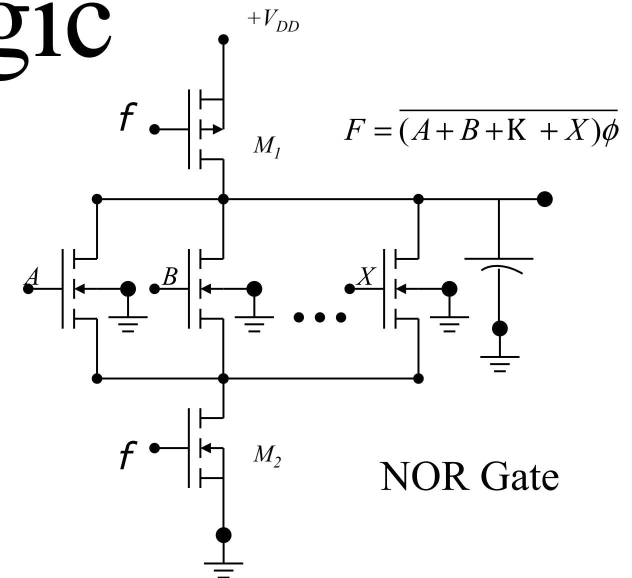
$$Nside = NA \bullet NB$$

$$Pside = PA + PB$$

NAND Gate

A		B		NA	PA	NB	PB	Nside	Pside	v_o	
0	Low	0	Low	OFF	ON	OFF	ON	OFF	ON	High	1
0	Low	1	High	OFF	ON	ON	OFF	OFF	ON	High	1
1	High	0	Low	ON	OFF	OFF	ON	OFF	ON	High	1
1	High	1	High	ON	OFF	ON	OFF	ON	OFF	Low	0

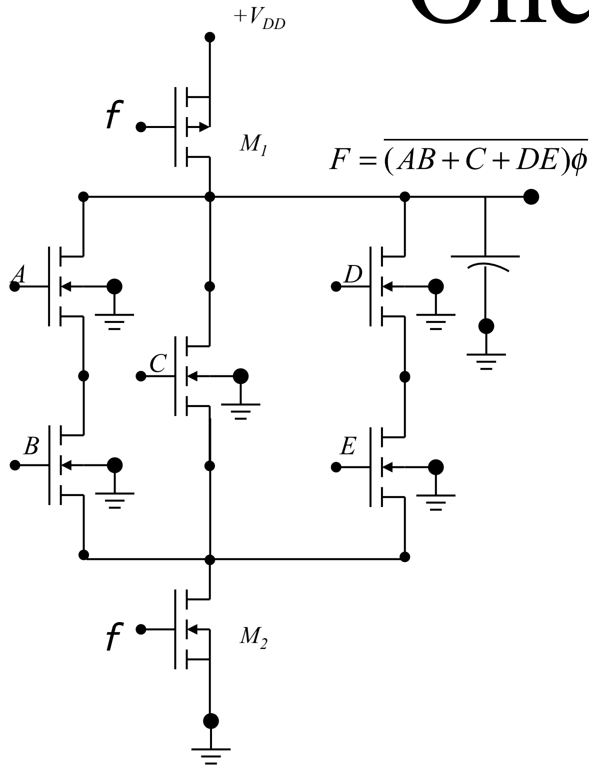
Dynamic Logic



- In this circuit, only when the clock, *f*, is high will the output be dependent on the inputs, *A, B, …X*.
- When *f* is low, M1 is ON, M2 is OFF and capacitor will be charged to VDD.
- When *f* is high, M1 is OFF, M2 is ON, and the capacitor will discharge through the NMOS transistors provided that at least on of the inputs is ON.

A		B		X		ϕ		NA	NB	NX	Nϕ	Pϕ	Nside	Pside	v_o	
0	Low	0	Low	0	Low	0	Low	OFF	OFF	OFF	OFF	ON	OFF	ON	High	1
0	Low	0	Low	1	High	0	Low	OFF	OFF	ON	OFF	ON	OFF	ON	High	1
0	Low	1	High	0	Low	0	Low	OFF	ON	OFF	OFF	ON	OFF	ON	High	1
0	Low	1	High	1	High	0	Low	OFF	ON	ON	OFF	ON	OFF	ON	High	1
1	High	0	Low	0	Low	0	Low	ON	OFF	OFF	OFF	ON	OFF	ON	High	1
1	High	0	Low	1	High	0	Low	ON	OFF	ON	OFF	ON	OFF	ON	High	1
1	High	1	High	0	Low	0	Low	ON	ON	OFF	OFF	ON	OFF	ON	High	1
1	High	1	High	1	High	0	Low	ON	ON	ON	OFF	ON	OFF	ON	High	1
0	Low	0	Low	0	Low	1	High	OFF	OFF	OFF	ON	OFF	OFF	OFF	High	1
0	Low	0	Low	1	High	1	High	OFF	OFF	ON	ON	OFF	ON	OFF	Low	0
0	Low	1	High	0	Low	1	High	OFF	ON	OFF	ON	OFF	ON	OFF	Low	0
0	Low	1	High	1	High	1	High	OFF	ON	ON	ON	OFF	ON	OFF	Low	0
1	High	0	Low	0	Low	1	High	ON	OFF	OFF	ON	OFF	ON	OFF	Low	0
1	High	0	Low	1	High	1	High	ON	OFF	ON	ON	OFF	ON	OFF	Low	0
1	High	1	High	0	Low	1	High	ON	ON	OFF	ON	OFF	ON	OFF	Low	0
1	High	1	High	1	High	1	High	ON	ON	ON	ON	OFF	ON	OFF	Low	0

One More Example



- Using this design, we can design other logic functions.

								A	B	C	D	E	P	N		
ϕ	A	B	C	D	E	M2	M1	NA	NB	NC	NC	NE	(NA*NB+NC+ND*NE)M2	M1	F	
1	0	0	0	0	0	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	1
1	0	0	0	0	1	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	ON	1
1	0	0	0	1	0	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	1
1	0	0	0	1	1	ON	OFF	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	0
1	0	0	1	0	0	ON	OFF	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	0
1	0	0	1	0	1	ON	OFF	OFF	OFF	ON	OFF	ON	ON	OFF	OFF	0
1	0	0	1	1	0	ON	OFF	OFF	OFF	ON	ON	OFF	ON	OFF	OFF	0
1	0	0	1	1	1	ON	OFF	OFF	OFF	ON	ON	ON	ON	OFF	OFF	0
1	0	1	0	0	0	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	ON	1
1	0	1	0	0	1	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	ON	1
1	0	1	0	1	0	ON	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	ON	1
1	0	1	0	1	1	ON	OFF	OFF	ON	OFF	ON	ON	ON	OFF	OFF	0
1	0	1	1	0	0	ON	OFF	OFF	ON	ON	OFF	OFF	ON	OFF	OFF	0
1	0	1	1	0	1	ON	OFF	OFF	ON	ON	OFF	ON	ON	OFF	OFF	0
1	0	1	1	1	0	ON	OFF	OFF	ON	ON	ON	OFF	ON	OFF	OFF	0
1	0	1	1	1	1	ON	OFF	OFF	ON	ON	ON	ON	ON	OFF	OFF	0
1	1	0	0	0	0	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON	1
1	1	0	0	0	1	ON	OFF	ON	OFF	OFF	OFF	ON	OFF	OFF	ON	1
1	1	0	0	1	0	ON	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	ON	1
1	1	0	0	1	1	ON	OFF	ON	OFF	OFF	ON	ON	ON	OFF	OFF	0
1	1	0	1	0	0	ON	OFF	ON	OFF	ON	OFF	OFF	ON	OFF	OFF	0
1	1	0	1	0	1	ON	OFF	ON	OFF	ON	OFF	ON	ON	OFF	OFF	0
1	1	0	1	1	0	ON	OFF	ON	OFF	ON	ON	OFF	ON	OFF	OFF	0
1	1	0	1	1	1	ON	OFF	ON	OFF	ON	ON	ON	ON	OFF	OFF	0
1	1	1	0	0	0	ON	OFF	ON	ON	OFF	OFF	OFF	ON	OFF	OFF	0
1	1	1	0	0	1	ON	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF	0
1	1	1	0	1	0	ON	OFF	ON	ON	OFF	ON	OFF	ON	OFF	OFF	0
1	1	1	0	1	1	ON	OFF	ON	ON	OFF	ON	ON	ON	OFF	OFF	0
1	1	1	1	0	0	ON	OFF	ON	ON	ON	OFF	OFF	ON	OFF	OFF	0
1	1	1	1	0	1	ON	OFF	ON	ON	ON	OFF	ON	ON	OFF	OFF	0
1	1	1	1	1	0	ON	OFF	ON	ON	ON	ON	OFF	ON	OFF	OFF	0
1	1	1	1	1	1	ON	OFF	ON	ON	ON	ON	ON	ON	OFF	OFF	0

Homework

- NMOS Transistors
  - Problems: 5.3, 5.4, 5.6
- Load-line Analysis
  - Problems: 5.14-17
- JFETs
  - Problems: 5.56, 5.57, 5.65
- CMOS
  - Problems: 6.48-6.50 6.69-6.70, 6.71-73