CIS 251-101 Computer Organization	**Homework 3** **Due: Week 10, Thurs. Nov. 4**	Dr. David Nassimi Fall 2004

TA: Ankur Gupta; **Hours:** W,Th 4:30-5:30; **Room:** ITC 2404; **Email:** AG59@njit.edu

Combinational Circuits Design, and Arithmetic

Study: Ch. 3, Sec. 3.3, pp. 104-110. (Design Examples)
Ch. 4, Sec. 4.3-4.6, pp. 147-176. (Decoders, Encoders, Multiplexers)
Ch. 5, pp. 201-229. (Arithmetic)

1. Consider the design of a 2-bit adder. The inputs are 2-bit unsigned integers $X = (X_1, X_0)$ and $Y = (Y_1, Y_0)$. (For this problem, assume the carry into the least-significant bit is 0.) The outputs are the sum, $S = (S_1, S_0)$ and output carry, C_2. (This is the carry out of bit 1.)

   (a) Show the design using a Half-Adder (HA) and a Full-Adder (FA).
   (Hint: Since $C_0 = 0$, you can use a HA for bit 0.)
   What is the total delay? (Assume a 2-input XOR gate has one gate delay. The sum bit inside the FA unit has to be implemented with two XOR gates.)

   (b) Show the design using only HA units. What is the total delay?

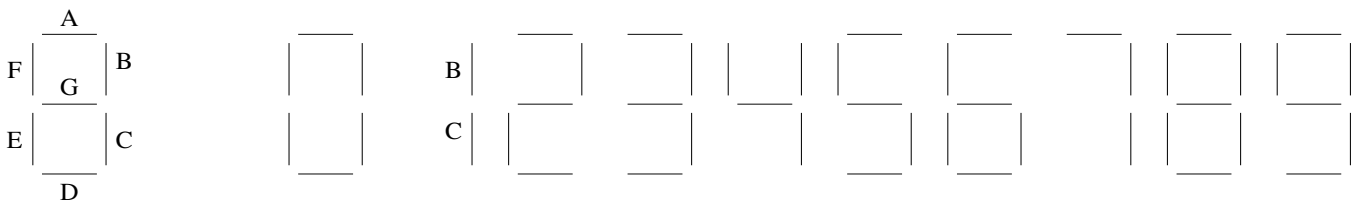
   (c) Use maps to obtain a 2-level AND-OR circuit for the adder. (Hint: Use a map for each output C_2, S_1, S_0.)

   (d) Design the adder using a 4-to-16 decoder, plus a few gates.

2. Construct a 4-to-16 decoder using two 2-to-4 decoders and a number of 2-input AND gates.

3. A word-multiplexer has two 4-bit word inputs: $A = (A_3, A_2, A_1, A_0)$ and $B = (B_3, B_2, B_1, B_0)$, and a select input S. ($S = 0$ selects A and $S = 1$ selects B.) Draw the complete circuit.

4. A *seven-segment-display* circuit receives as input a BCD digit (W, X, Y, Z), where W is the most-significant-bit, and input values of 10 through 15 are "don't cares". The circuit has seven outputs: A, B, C, D, E, F, G. The value of 1 on each output will turn ON the corresponding light segment. The proper display of digits 0 through 9 are shown below.

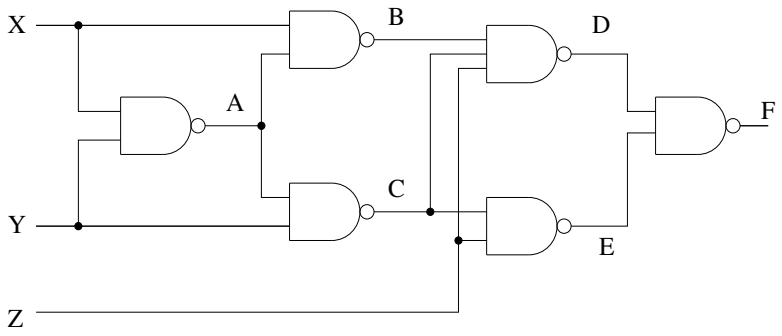


   (a) Complete the design using Karnaugh maps. (For each output, use a map to obtain a simplified sum-of-products expression.) Draw the complete 2-level AND-OR circuit. (Assume that the complements of the input variables are also available as input.)

   (b) Repeat the design of seven-segment-display using a decoder and a number of OR or NOR gates.
   (Hint: A NOR gate may be used to implement a function in terms of its maxterms. This is appropriate when the function has only a few maxterms and many minterms.)

5. Consider the NAND circuit in the following diagram. Obtain a simplified sum-of-products expression for the output F. Then, draw the simplified 2-level NAND circuit for the output F.

   Hint: You may use a truth table to compute F, then use a map to obtain a simplified sum-of-products expression for F. Alternatively, you may use the algebraic method to find an expression for F and then simplify.



(a) NAND circuit to be simplified

Additional Exercises (Not to be handed-in)

6. A *majority* function of four variable, $f(A, B, C, D)$, has a value 1 when three or more inputs are 1.

   (a) Using the truth table, find the sum-of-minterms for this function.

   (b) Starting with the sum-of-minterms expression, and using algebraic manipulations, obtain a simplified sum-of-products form.

   (c) Using a Karnaugh map, obtain a simplified sum-of-products form.

   (d) Implement the function using a minimal 2-level NAND circuit.

7. A comparator circuit has two 2-bit integer inputs $A = (A_1, A_0)$ and $B = (B_1, B_0)$. (A_0 and B_0 are the least significant bits of A and B. The inputs A and B are unsigned integers in the range 0 through 3.) The circuit compares A and B and produces the result by two outputs:

   S (smaller): This output will be 1 when $A < B$.
   G (greater): This output will be 1 when $A > B$.

   (If $A = B$ then both S and G will be 0.)

   Design this circuit using maps. Draw the complete two-level AND-OR circuit.