Moore’s Law

- In 1965, Gordon Moore noted that the number of transistors on a chip doubled every 18 to 24 months.

- He made a prediction that semiconductor technology will double its effectiveness every 18 months.
Moore’s Law

Electronics, April 19, 1965.
Evolution in Complexity
Transistor Counts

1 Billion Transistors

Source: Intel

courtesy, Intel
Moore’s law in Microprocessors

2X growth in 1.96 years!

Transistors on Lead Microprocessors double every 2 years

Courtesy, Intel
Die Size Growth

Die size grows by 14% to satisfy Moore’s Law

~7% growth per year
~2X growth in 10 years
**Microprocessor scaling**  

**Lead designs** are fundamentally new designs. They typically add new features that require more transistors and therefore a larger die size.

**Compactions** change completed designs to make them work on new fabrication processes. This allows for higher frequency, lower power, and smaller dies.
Microprocessor scaling

Each new lead design offers increased performance from added functionality but uses a bigger die size than a compaction in the same generation. It is the improvements in frequency and reductions in cost that come from compacting the design onto future process generations that make the new designs profitable.

<table>
<thead>
<tr>
<th>Year</th>
<th>Technology node (nm)</th>
<th>$L_{\text{GATE}}$ (nm)</th>
<th>$T_{\text{OX-F}}$ (nm)</th>
<th>$V_{\text{dd}}$ (V)</th>
<th>Metal layers</th>
</tr>
</thead>
<tbody>
<tr>
<td>1993</td>
<td>500</td>
<td>500</td>
<td>8.0</td>
<td>3.3</td>
<td>4</td>
</tr>
<tr>
<td>1995</td>
<td>350</td>
<td>350</td>
<td>5.2</td>
<td>2.5</td>
<td>4</td>
</tr>
<tr>
<td>1997</td>
<td>250</td>
<td>200</td>
<td>3.1</td>
<td>1.8</td>
<td>5</td>
</tr>
<tr>
<td>1999</td>
<td>180</td>
<td>130</td>
<td>2.0</td>
<td>1.6</td>
<td>6</td>
</tr>
<tr>
<td>2001</td>
<td>130</td>
<td>70</td>
<td>1.4</td>
<td>1.4</td>
<td>6</td>
</tr>
<tr>
<td>2003</td>
<td>90</td>
<td>50</td>
<td>1.2</td>
<td>1.2</td>
<td>7</td>
</tr>
</tbody>
</table>

On average the semiconductor industry has begun a new generation of fabrication process every 2 to 3 years. Each generation reduces horizontal dimensions about 30 percent compared to the previous generation. It would be possible to produce new generations more often if a smaller shrink factor was used, but a smaller improvement in performance might not justify the expense of new equipment. A larger shrink factor could provide more performance improvement but would require a longer time between generations. The company attempting the larger shrink factor would be at a disadvantage when competitors had advanced to a new process before them.
Small incremental improvements are constantly being made to the process that allow for part of the steady improvement in processor frequency. As a result, a compaction microprocessor design may first ship at about the same frequency as the previous generation, which has been gradually improving since its launch.
Doubles every 2 years

Lead Microprocessors frequency doubles every 2 years

Courtesy, Intel
Lead Microprocessors power continues to increase

Courtesy, Intel
Power will be a major problem

Power delivery and dissipation will be prohibitive

Courtesy, Intel
Power density too high to keep junctions at low temp

Courtesy, Intel
Not Only Microprocessors

Cell Phone

Digital Cellular Market
(Phones Shipped)

<table>
<thead>
<tr>
<th>Year</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>1996</td>
<td>48M</td>
</tr>
<tr>
<td>1997</td>
<td>86M</td>
</tr>
<tr>
<td>1998</td>
<td>162M</td>
</tr>
<tr>
<td>1999</td>
<td>260M</td>
</tr>
<tr>
<td>2000</td>
<td>435M</td>
</tr>
</tbody>
</table>

(data from Texas Instruments)
Challenges in Digital Design

α DSM

“Microscopic Problems”
- Ultra-high speed design
- Interconnect
- Noise, Crosstalk
- Reliability, Manufacturability
- Power Dissipation
- Clock distribution.

Everything Looks a Little Different

α 1/DSM

“Macroscopic Issues”
- Time-to-Market
- Millions of Gates
- High-Level Abstractions
- Reuse & IP: Portability
- Predictability
- etc.

...and There’s a Lot of Them!
Productivity Trends

Complexity outpaces design productivity

Source: Sematech

Courtesy, ITRS Roadmap
**Abstraction** is used to manage complexity of design

- Hide details that are not important

<table>
<thead>
<tr>
<th>Application Software</th>
<th>Programs</th>
</tr>
</thead>
<tbody>
<tr>
<td>Compiler</td>
<td>Device Drivers</td>
</tr>
<tr>
<td>Operating Systems</td>
<td>Instructions</td>
</tr>
<tr>
<td>Architecture</td>
<td>Registers</td>
</tr>
<tr>
<td>Micro-architecture</td>
<td>Datapaths</td>
</tr>
<tr>
<td>Logic</td>
<td>Controllers</td>
</tr>
<tr>
<td>Digital circuits</td>
<td>Adders</td>
</tr>
<tr>
<td>Analog circuits</td>
<td>Memories</td>
</tr>
<tr>
<td>Devices</td>
<td>AND gates</td>
</tr>
<tr>
<td>Physics</td>
<td>NOT gates</td>
</tr>
<tr>
<td></td>
<td>Amplifiers</td>
</tr>
<tr>
<td></td>
<td>Filters</td>
</tr>
<tr>
<td></td>
<td>Transistors</td>
</tr>
<tr>
<td></td>
<td>Diodes</td>
</tr>
<tr>
<td></td>
<td>Electrons</td>
</tr>
</tbody>
</table>
Domains and Levels of Modeling

“Y-chart” from Gajski & Kuhn
Domains and Levels of Modeling

"Y-chart" from Gajski & Kahn
Domains and Levels of Modeling

Structural

Functional

Geometric

Polygons

Sticks

Standard Cells

Floor Plan

“Y-chart” from Gajski & Kahn

Domains and Levels of Modeling

Structural

Functional

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“Y-chart” from Gajski & Kahn
unified product development system makes high levels of design abstraction effective through the entire design process. This revolutionizes the way products can be created and opens embedded design to both hardware and software engineers.
Cost per Transistor

Fabrication capital cost per transistor (Moore’s law)
A look at Moore’s Law in action

- **Price per Transistor (Billionths of $1)**
- **Transistors Made per Year**

Data Source: VLSI Research
Moore’s Law Facts

• **In 2014**, semiconductor production facilities made some 250 billion billion (250 \( \times 10^{18} \)) transistors.

• Every second of that year, on average, 8 trillion transistors were produced.

• That figure is about 25 times the [number of stars in the Milky Way](https://en.wikipedia.org/wiki/Number_of_stars_in_the_Milky_Way) and some 75 times the [number of galaxies](https://en.wikipedia.org/wiki/Number_of_galaxies) in the [known universe](https://en.wikipedia.org/wiki/Universe).

• The rate of growth has also been extraordinary. More transistors were made in 2014 than in all the years prior to 2011.

• The collective pursuit of Moore’s Law has driven this growth. For decades, manufacturing innovation and simple miniaturization have enabled engineers to pack more capability into the same area of silicon. The result has been a steady decrease in manufacturing cost per transistor.

• This steady, predictable decline in prices was a self-reinforcing gift. Because electronics manufacturers could depend on Moore’s Law, they could plan further ahead and invest more in the development of new and better-performing products. In ways profound and surprising, this situation promoted economic growth.
**The future of Moore's law**

No exponential trend can continue forever, and this simple fact has led to predictions of the end of Moore's law for decades. All these predictions have turned out to be wrong. For 30 years, there have always been seemingly insurmountable problems about 10 years in the future. Perhaps one of the most important lessons of Moore's law is that when billions of dollars in profits are on the line, incredibly difficult problems can be overcome.

Is Moore’s Law dead? No, not yet. But it can’t go on forever. The number of transistors on a chip has doubled about every two years for almost five decades. Smaller transistors can fit into smaller spaces, making it possible to put more circuitry on the same size or a smaller chip. We also have seen higher digital speeds, high-frequency RF circuitry, lower power consumption, and lower costs. But as devices get smaller, we approach the atomic level of the materials, meaning the downward scaling will come to an end.

Right now we are at the 22-nm node with 14 nm in the wings. Some companies are even working on the 7-nm node and perhaps one or two more nodes at 5 nm or 3.5 nm are possible, but not without some major changes.

New architectures and geometries have emerged in response. The new circuitry is more 3D or vertical. Imec’s smaller FinFET design enables CMOS at the 22-nm level. Also, indium gallium arsenide (InGaAs) or indium phosphide (InP) can be used with the silicon to make the transistor faster and smaller. IBM is exploring the use of InGaAs with silicon germanium (SiGe) to produce smaller and faster CMOS devices. Chip-stacking techniques offer some promise as well. Such techniques could help scale CMOS down to the 7-nm node. Are you ready for 0.5-V dc supply voltages and 200- to 300-mV thresholds?
Clearly, dimensional scaling is no longer associated with lower average cost per transistor. The chart below, published by IBS about a year ago, shows the diminishing benefit of cost reduction from dimensional scaling. In fact, the chart indicates that the 20nm node might be associated with higher cost than the previous node.

But that’s not all. New processes are also necessary. To date, the biggest factor in limiting the downward scaling has been the photolithography process that translates the design patterns into the masks that are used in deposition and etching. Immersion lithography and double patterning have helped, but the ultimate solution appears to be extreme ultraviolet (EUV) lithography. EUV has been in the works for years and is still not ready. It is expected to be available in 2015 and beyond.

Another development is the trend to 450-mm wafers from the current 300-mm size. This will offer pricing advantages, like the 200-mm to 300-mm wafer transition did. But the transition to 450-mm wafers will require all new fab tools, which is expensive. The way things are going, you may not see 450 mm until 2018 or beyond.

Intel is readying 14-nanometer process technology for chips due out next year and sees a path all the way to 5nm processors by the end of the decade.

The immersion lithography Intel currently uses to fabricate 22nm chips is also likely to remain in use for a couple more generations. Bohr said a next-generation technology called extreme ultraviolet (EUV) lithography would be preferable for the 10nm node, but it probably wouldn't be cost-effective at that point.
## Some Examples (1994)

<table>
<thead>
<tr>
<th>Chip</th>
<th>Metal layers</th>
<th>Line width</th>
<th>Wafer cost</th>
<th>Def./cm²</th>
<th>Area mm²</th>
<th>Dies/wafer</th>
<th>Yield</th>
<th>Die cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>386DX</td>
<td>2</td>
<td>0.90</td>
<td>$900</td>
<td>1.0</td>
<td>43</td>
<td>360</td>
<td>71%</td>
<td>$4</td>
</tr>
<tr>
<td>486 DX2</td>
<td>3</td>
<td>0.80</td>
<td>$1200</td>
<td>1.0</td>
<td>81</td>
<td>181</td>
<td>54%</td>
<td>$12</td>
</tr>
<tr>
<td>Power PC 601</td>
<td>4</td>
<td>0.80</td>
<td>$1700</td>
<td>1.3</td>
<td>121</td>
<td>115</td>
<td>28%</td>
<td>$53</td>
</tr>
<tr>
<td>HP PA 7100</td>
<td>3</td>
<td>0.80</td>
<td>$1300</td>
<td>1.0</td>
<td>196</td>
<td>66</td>
<td>27%</td>
<td>$73</td>
</tr>
<tr>
<td>DEC Alpha</td>
<td>3</td>
<td>0.70</td>
<td>$1500</td>
<td>1.2</td>
<td>234</td>
<td>53</td>
<td>19%</td>
<td>$149</td>
</tr>
<tr>
<td>Super Sparc</td>
<td>3</td>
<td>0.70</td>
<td>$1700</td>
<td>1.6</td>
<td>256</td>
<td>48</td>
<td>13%</td>
<td>$272</td>
</tr>
<tr>
<td>Pentium</td>
<td>3</td>
<td>0.80</td>
<td>$1500</td>
<td>1.5</td>
<td>296</td>
<td>40</td>
<td>9%</td>
<td>$417</td>
</tr>
</tbody>
</table>
The following Nvidia chart provides the first order explanation. The cost reduction of dimensional scaling results from doubling the number of transistors per wafer. But if the wafer cost of the new technology node increases by too much, then it neutralizes the original cost reduction. The Nvidia chart shows the wafer cost of recent nodes over time.

In the past (...80nm, 55nm, 40nm), the incremental wafer cost increases were small, and rapid depreciation of those costs resulted in almost constant average wafer price. Recent nodes (28nm, 20nm, 14nm...), however, signal a new reality.

The evolution of computers has been characterized by increasing processor speed, decreasing component size, increasing memory size, and increasing I/O capacity and speed.

- One factor responsible for the great increase in processor speed is the shrinking size of microprocessor components; this reduces the distance between components and hence increases speed. However, the true gains in speed in recent years have come from the organization of the processor, including heavy use of pipelining and parallel execution techniques and the use of speculative execution techniques (tentative execution of future instructions that might be needed). All of these techniques are designed to keep the processor busy as much of the time as possible.

- A critical issue in computer system design is balancing the performance of the various elements so that gains in performance in one area are not handicapped by a lag in other areas. In particular, processor speed has increased more rapidly than memory access time. A variety of techniques is used to compensate for this mismatch, including caches, wider data paths from memory to processor, and more intelligent memory chips.
Beyond 10nm, Intel has pegged 7nm and 5nm transistors as the next stops on the Moore's Law-driven path to ever-smaller circuitry packed more densely onto computer chips every 18 months or so. Of course, those tiny transistors may not actually be made of silicon at that point.

Intel's technology pipeline is full with research extending out 10 years and down to the 10nm, 7nm, and 5nm nodes. It looks like they have a solution for 10nm and hopefully they will have solutions for 7nm and 5nm.
Summary

• Digital integrated circuits have come a long way and still have quite some potential left for the coming decades

• Some interesting challenges ahead
  – Getting a clear perspective on the challenges and potential solutions is the purpose of this book

• Understanding the design metrics that govern digital design is crucial
  – Cost, reliability, speed, power and energy dissipation