Minimum Linewidth Trends

Sources: Intel, SRi International, SCS
Semiconductor Process (node) Size

All semiconductor devices are manufactured as a series of very thin, stacked layers on some substrate material (normally silicon dioxide). Each layer is created from a different mask, and different layers can be made of different materials.

The masks used to create each layer are basically like a 1-bit bitmap: they have a grid of squares (similar to pixels) that are either "on" or "off".

The process size defines lambda, which is how large each of those squares will be on the chip.

The properties of semiconductor devices, like other electronic devices, are based on the relative sizes of their dimensions.

For example, a resistor that is made of a 4 lambda x 20 lambda rectangle will have essentially the same resistance for any value of lambda.
Dimensional Scaling

At a high-level abstraction, you can assume that each layer has zero thickness. However, layers have non-zero thickness, and their thickness doesn't scale to perfectly match when you change your value of lambda.
If you move to a smaller value of lambda (a smaller process node), interesting things can happen. For example, the capacitance of a capacitor is directly proportional to the area of the plates, and inversely proportional to the distance between them.
If you divide lambda in half, you divide the area of the plates by four. Unless you also divide the thickness of the layer(s) between the plates by four, you will end up with a capacitor with lower capacitance.

This is good for making transistors because they have capacitance between their terminals which cuts back on increasing the switching frequency of those transistors. Also, the dynamic power a transistor consumes (when switching) is proportional to capacitance. So smaller transistors scale more easily to higher frequencies, and use less power.
Smaller transistors have lower "turn on" voltages, which means they can be driven by lower voltages (core voltages). And dynamic power loss in a transistor is proportional to the square of that voltage; cut the voltage in half, cut power consumption by a factor of four.
Minimum Linewidth Trends

Fig. 3. Comparison of ITRS 2007 and 2008 Update for the trends of printed (resist) and physical gate lengths.

# Minimum Feature Size

<table>
<thead>
<tr>
<th>Year</th>
<th>Processor</th>
<th>Speed</th>
<th>Transistors</th>
<th>Process</th>
</tr>
</thead>
<tbody>
<tr>
<td>1982</td>
<td>i286</td>
<td>6 - 25 MHz</td>
<td>~134,000</td>
<td>1.5 µm</td>
</tr>
<tr>
<td>1986</td>
<td>i386</td>
<td>16 – 40 MHz</td>
<td>~270,000</td>
<td>1 µm</td>
</tr>
<tr>
<td>1989</td>
<td>i486</td>
<td>16 – 133 MHz</td>
<td>~1 million</td>
<td>.8 µm</td>
</tr>
<tr>
<td>1993</td>
<td>Pentium</td>
<td>60 - 300 MHz</td>
<td>~3 million</td>
<td>.6 µm</td>
</tr>
<tr>
<td>1995</td>
<td>Pentium Pro</td>
<td>150 - 200 MHz</td>
<td>~4 million</td>
<td>.5 µm</td>
</tr>
<tr>
<td>1997</td>
<td>Pentium II</td>
<td>233 - 450 MHz</td>
<td>~5 million</td>
<td>.35 µm</td>
</tr>
<tr>
<td>1999</td>
<td>Pentium III</td>
<td>450 – 1400 MHz</td>
<td>~10 million</td>
<td>.25 µm</td>
</tr>
<tr>
<td>2000</td>
<td>Pentium 4</td>
<td>1.3 – 3.8 GHz</td>
<td>~50 million</td>
<td>.18 µm</td>
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<tr>
<td>2005</td>
<td>Pentium D</td>
<td>2 cores/package</td>
<td>~200 million</td>
<td>.09 µm</td>
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<td>2006</td>
<td>Core 2</td>
<td>2 cores/die</td>
<td>~300 million</td>
<td>.065 µm</td>
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<tr>
<td>2008</td>
<td>Core i7</td>
<td>4 cores/die</td>
<td>~800 million</td>
<td>.040 µm</td>
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<tr>
<td>2010</td>
<td>“Sandy Bridge”</td>
<td>8 cores/die</td>
<td>??</td>
<td>.032 µm</td>
</tr>
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</table>
Current Issues

Si Nanowire
- Control of wire surface property
- Source Drain contact
- Optimization of wire diameter
- Compact I-V model

III-V & Ge Nanowire
- High-k gate insulator
- Wire formation technique

CNT:
- Growth and integration of CNT
- Width and Chirality control
- Chirality determines conduction types: metal or semiconductor

Graphene:
- Graphene formation technique
- Suppression of off-current
  - Very small bandgap or no bandgap (semi-metal)
- Control of ribbon edge structure which affects bandgap

Fig. 19. Long range roadmap for logic CMOS transistors for next 30 years.
We do know system and algorithms are important!
But do not know how it can be by us for use of bio?

Fig. 20. Further long range roadmap in this century.
Semiconductor Manufacturing
3 Major Material Types

- Insulators – Materials which block or resist the flow of electric current. An example of an insulator would be Silicon Dioxide (SiO$_2$) which has a resistivity of $10^{14} - 10^{16}$ ohm-cm.

- Conductors – Materials which readily support the flow of electric current. An example of a conductor would be aluminum which has a resistivity of $2.7 \times 10^{-6}$ ohm-cm.

- Semiconductors – A material which can be made to act as an insulator or act as a conductor. An example of a semiconductor would be silicon with an intrinsic resistivity of $2.3 \times 10^5$ ohm-cm and where doped silicon can have resistivities down to $1 \times 10^{-4}$ ohm-cm.
Periodic Table Group III – IV elements

- Silicon is an elemental semiconductor material because of four valence shell electrons. It occurs in nature as silica and is refined and purified to make wafers.

- Pure silicon is intrinsic silicon. The silicon atoms bond together in covalent bonds, which defines many of silicon’s properties. Silicon atoms bond together in set, repeatable patterns, referred to as a crystal.

- Germanium was the first semiconductor material used to make chips, but it was soon replaced by silicon. The reasons for this change are:
  Abundance of silicon, Higher melting temperature for wider processing range, wide temperature range during semiconductor usage

  Natural growth of silicon dioxide
  - Silicon dioxide (SiO2) is a high quality, stable electrical insulator material that also serves as a good chemical barrier to protect silicon from external contaminants. The ability to grow stable, thin SiO2 is fundamental to the fabrication of Metal-Oxide-Semiconductor (MOS) devices.

- Doping increases silicon conductivity by adding small amounts of other elements. Common dopant elements are from trivalent, p-type Group IIIA (boron) and pentavalent, n-type Group VA (phosphorus, arsenic and antimony).

- It is the junction between the n-type and p-type doped regions (referred to as a pn junction) that permit silicon to function as a semiconductor.
The alternative semiconductor materials are primarily the compound semiconductors. They are formed from Group IIIA and Group VA (referred to as III-V compounds). An example is gallium arsenide (GaAs).

Some alternative semiconductors come from Group IIA and VIA, referred to as II-VI compounds.

GaAs is the most common III-V compound semiconductor material. GaAs ICs have greater electron mobility, and therefore are faster than ICs made with silicon. GaAs ICs also have higher radiation hardness than silicon, which is better for space and military applications. The primary disadvantage of GaAs is the lack of a natural oxide.

GaN is a binary III/V direct bandgap semiconductor commonly used in bright light-emitting diodes since the 1990s. Because GaN transistors can operate at much higher temperatures and work at much higher voltages than gallium arsenide (GaAs) transistors, they make ideal power amplifiers at microwave frequencies.

The advantages of GaN devices include high output power with small physical volume, and high efficiency in power amplifiers at ultra-high and microwave radio frequencies.

The main problem with GaN technology is cost. A special process is required to grow a GaN crystal or wafer on which transistors and integrated circuits (ICs) can be fabricated. Once the process is implemented on a large scale, the cost should come down.
Material States

Crystalline (Silicon Wafers)

Amorphous (Oxide, Nitride)

Polycrystalline (Polysilicon)
Typical Insulators

- Silicon Dioxide (SiO$_2$) – The most common insulator in Silicon Integrated Circuits. Silicon Dioxide is a good barrier materials with excellent electrical properties.

- Silicon Nitride (Ni$_3$N$_4$) – Frequently used as a barrier or final passivation layer for Silicon Integrated Circuits. Silicon Nitride is an excellent barrier, although Silicon Nitride exhibits too much stress to be in direct contact with Silicon.
Typical Conductors

• Aluminum – Most frequently used conductor for Silicon Integrated Circuits.

• Titanium, Cobalt, Nickel and Platinum – Metals commonly used to form silicide contacts to Silicon.

• Tungsten – Used for plug filling.

• Titanium Nitride – Used as a barrier layer to prevent metal from interacting or to prevent metals and silicon from interacting.

• Copper – Now used as a conductor.
Silicon “Doping”

Wafer doping is the introduction of a dopant into the crystal structure of a semiconductor material to modify its electronic properties. In advanced fabs, this is done primarily by ion implantation. The early doping method was thermal diffusion.

Doping Levels

<10^{-14} to <10^{19} \text{ atoms/cm}^3

<.01 to >1000 \text{ ppm}
Active Component Structures

• Active components, such as diodes and transistors can be used to control the direction of current flow. PN junction diodes are formed when there is a region of n-type semiconductor adjacent to a region of p-type semiconductor. A difference in charge at the pn junction creates a depletion region that results in a barrier voltage that must be overcome before a diode can be operated. A bias voltage can be configured to have a reverse bias, with little or no conduction through the diode, or with a forward bias, which permits current flow.

• The bipolar junction transistor (BJT) has three electrodes and two pn junctions. A BJT is configured as an npn or pnp transistor and biased for conduction mode. It is a current-amplifying device.

• A schottky diode is formed when metal is brought in contact with a lightly doped n-type semiconductor material. This diode is used in faster and more power efficient BJT circuits.

• The field-effect transistor (FET), a voltage-amplifying device, is more compact and power efficient than BJT devices. A thin gate oxide located between the other two electrodes of the transistor insulates the gate on the MOSFET. There are two categories of MOSFETs, nMOS (n-channel) and pMOS (p-channel), each which is defined by its majority current carriers. There is a biasing scheme for operating each type of MOSFET in conduction mode.

• BiCMOS technology makes use of the best features of both CMOS and bipolar technology in the same IC device.
Bipolar Transistor

Discrete Transistor

Integrated Circuit Transistor

[Diagram showing the differences between discrete and integrated circuit transistors, with labels for Base, Emitter, Collector, N+ Substrate, N Epi, Deep N+, N+ Buried Layer, P Substrate, P+ Iso.]
MOSFETs

- Metal-poly-Oxide-Semiconductor structures built onto substrate
  - *Diffusion*: Inject dopants into substrate
  - *Oxidation*: Form layer of SiO2 (glass)
  - *Deposition* and *etching*: Add aluminum/copper wires
MOS Inverter

N-Transistor

Gate = Control Input – Affects Flow of Electricity Between Drain & Source

SYMBOLS

0 = Gate Off
1 = Gate On

When gate is on:
Passing a “0” = Good
Passing a “1” = Poor

Due to Transistor Saturation Effects

0 = Gate On
1 = Gate Off

When gate is on:
Passing a “0” = Poor
Passing a “1” = Good

Complementary CMOS Switches Combine an N-Switch & P-Switch
CMOS Inverter

\[ T = H \bar{I}_2 \]

crowbarred = both pull up + down simultaneously. Indeterminate logic level. Excess power dissipated.
MOS Versus Bipolar

• MOS is simpler to produce than Bipolar. The minimum number of masks to make Bipolar is seven, and the minimum number of masks to make MOS is five.

• MOS requires less drive current. MOS devices are voltage controlled with high impedance inputs. Bipolar devices are current controlled with low impedance input.

• MOS dissipates less power. This is particularly true of CMOS logic which only draws power when switching states.

• MOS devices are simpler to isolate and can be packed more tightly.

• As we have seen, MOS has become the dominant technology.
IC Manufacturing

- Silicon ingot
  - Slicer
  - Blank wafers
    - 20 to 40 processing steps
  - Tested dies
    - Dicer
    - Tested wafer
      - Wafer tester
        - Patterned wafers
  - Bond die to package
    - Packaged dies
      - Tested packaged dies
        - Part tester
          - Ship to customers
IC Fabrication

- Chips are fabricated using set of masks
  - Photolithography

- Basic steps
  - oxidize
  - apply photoresist
  - remove photoresist with mask
  - HF acid eats oxide but not photoresist
  - pirana acid eats photoresist
  - ion implantation (diffusion, wells)
  - vapor deposition (poly)
  - plasma etching (metal)
Semiconductor Manufacturing Processes

- Design
- Wafer Preparation
- Front-end Processes
- Photolithography
- Etch
- Cleaning
- Thin Films
- Ion Implantation
- Planarization
- Test and Assembly

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Wafer Preparation | 29 - 34
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Photolithography | 43 - 50
Etch | 55 - 59
Cleaning | 60 - 62
Thin Films | 35 - 40
Ion Implantation | 51 - 54
Planarization | 63 - 68
Test and Assembly | 77
Design

- Establish Design Rules
- Circuit Element Design
- Interconnect Routing
- Device Simulation
- Pattern Preparation
Element Cell Library (Snap Togethern)
Wafer Preparation

- Polysilicon Refining
- Crystal Pulling
- Wafer Slicing & Polishing
- Epitaxial Silicon Deposition
**Sand / Ingot**

**Sand**
With about 25% (mass) Silicon is - after Oxygen - the second most frequent chemical element in the earth's crust. Sand - especially Quartz - has high percentages of Silicon in the form of Silicon dioxide (SiO$_2$) and is the base ingredient for semiconductor manufacturing.

**Melted Silicon**
- **scale: wafer level (~300mm / 12 inch)**
Silicon is purified in multiple steps to finally reach semiconductor manufacturing quality which is called Electronic Grade Silicon. Electronic Grade Silicon may only have one alien atom every one billion Silicon atoms. In this picture you can see how one big crystal is grown from the purified silicon melt. The resulting mono crystal is called Ingot.

**Mono-crystal Silicon Ingot**
- **scale: wafer level (~300mm / 12 inch)**
An ingot has been produced from Electronic Grade Silicon. One ingot weights about 100 kilograms (=220 pounds) and has a Silicon purity of 99.9999%.
Crystal Pulling

Process Conditions
Flow Rate: 20 to 50 liters/min
Time: 18 to 24 hours
Temperature: >1,300 degrees C
Pressure: 20 Torr

Materials
Polysilicon Nodules *
Ar *
H₂

* High proportion of the total product use
**Ingot Slicing**

scale: wafer level (~300mm / 12 inch)

The Ingot is cut into individual silicon discs called wafers.

**Wafer**

scale: wafer level (~300mm / 12 inch)

The wafers are polished until they have flawless, mirror-smooth surfaces. Intel buys those manufacturing ready wafers from third party companies. Intel’s highly advanced 45nm High-K/Metal Gate process uses wafers with a diameter of 300 millimeter (~12 inches). When Intel first began making chips, the company printed circuits on 2-inch (50mm) wafers. Now the company uses 300mm wafers, resulting in decreased costs per chip.
The silicon ingot is sliced into individual wafers, polished, and cleaned.
Wafer Manufacturing Process Overview

1) Pull Crystal Ingot

2) Grind Ingot to Diameter

3) Saw Off Ingot ends

4) Saw Up Ingot into Wafers - Damage ~75µm

5) Grind Round Edges Onto Wafers

6) Lap Wafers for Flatness - Damage ~ 12µm

7) Damage Removal Etch - Damage ~2µm

8) Mirror Polish Wafers - No Damage

9) Final Clean
Thin Films

- Chemical Vapor Deposition (CVD) Dielectric
- CVD Tungsten
- Physical Vapor Deposition (PVD)
- Chamber Cleaning
Chemical Vapor Deposition

- Chemical Vapor Deposition (CVD) thermally reacts gases to deposit films.

- CVD can be performed over a variety of temperatures from around 400°C on the low end to over 1,200°C on the high end.

- CVD films can be deposited over a variety of different material layers.

- Compared to oxidation, CVD films can be deposited at lower temperatures, can be deposited over material layers other than silicon and do not consume any of the underlying substrate material the way oxidation does.

- CVD can deposit a wide variety of Insulating, Conducting and Semiconducting films.
Chemical Vapor Deposition (CVD) Dielectric

Chemical Reactions
\[ \text{Si(OC}_2\text{H}_5\text{)}_4 + 9 \text{O}_3 \rightarrow \text{SiO}_2 + 5 \text{CO} + 3 \text{CO}_2 + 10 \text{H}_2\text{O} \]

Process Conditions (ILD)
- Flow Rate: 100 to 300 sccm
- Pressure: 50 Torr to Atmospheric

CVD Dielectric
- \( \text{O}_2 \)
- \( \text{O}_3 \)
- \( \text{TEOS}^* \)
- \( \text{TMP}^* \)

* High proportion of the total product use
Chemical Vapor Deposition (CVD) Tungsten

Chemical Reactions
\[ \text{WF}_6 + 3 \text{H}_2 \rightarrow \text{W} + 6 \text{HF} \]

Process Conditions
- Flow Rate: 100 to 300 sccm
- Pressure: 100 mTorr
- Temperature: 400 degrees C.

CVD Dielectric
- WF\(_6\) *
- Ar
- H\(_2\)
- N\(_2\)

* High proportion of the total product use
Physical Vapor Deposition (PVD)

Process Conditions
Pressure: < 5 mTorr
Temperature: 200 degrees C.
RF Power:

Barrier Metals
SiH₄
Ar
N₂
N₂
Ti PVD Targets *

* High proportion of the total product use
**Thin films - Epitaxial Silicon Deposition**

Chemical Reactions
Silicon Deposition: \( \text{HSiCl}_3 + \text{H}_2 \rightarrow \text{Si} + 3 \text{HCl} \)

Process Conditions
Flow Rates: 5 to 50 liters/min
Temperature: 900 to 1,100 degrees C.
Pressure: 100 Torr to Atmospheric

Silicon Sources
- SiH\(_4\)
- H\(_2\)SiCl\(_2\)
- HSiCl\(_3\) *
- SiCl\(_4\) *

Dopants
- AsH\(_3\)
- B\(_2\)H\(_6\)
- PH\(_3\)

Etchant
- HCl

Carriers
- Ar
- H\(_2\) *
- N\(_2\)

* High proportion of the total product use
Front-End Processes

- Thermal Oxidation
- Silicon Nitride Deposition
  - Low Pressure Chemical Vapor Deposition (LPCVD)
- Polysilicon Deposition
  - Low Pressure Chemical Vapor Deposition (LPCVD)
- Annealing
**Front-End Processes**

**Chemical Reactions**
- Thermal Oxidation: \( \text{Si} + \text{O}_2 \rightarrow \text{SiO}_2 \)
- Nitride Deposition: \( 3 \text{SiH}_4 + 4 \text{NH}_3 \rightarrow \text{Si}_3\text{N}_4 + 12 \text{H}_2 \)
- Polysilicon Deposition: \( \text{SiH}_4 \rightarrow \text{Si} + 2 \text{H}_2 \)

**Process Conditions (Silicon Nitride LPCVD)**
- Flow Rates: 10 - 300 sccm
- Temperature: 600 degrees C.
- Pressure: 100 mTorr

<table>
<thead>
<tr>
<th>Oxidation</th>
<th>Polysilicon</th>
<th>Nitride</th>
<th>Annealing</th>
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<tr>
<td>Ar</td>
<td>H(_2)</td>
<td>NH(_3) *</td>
<td>Ar</td>
</tr>
<tr>
<td>N(_2)</td>
<td>N(_2)</td>
<td>H(_2)SiCl(_2) *</td>
<td>He</td>
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<tr>
<td>H(_2)O</td>
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<td>N(_2)</td>
<td>H(_2)</td>
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<td>B(_2)H(_6)</td>
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<tr>
<td>HCl *</td>
<td>PH(_3)</td>
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<td></td>
</tr>
<tr>
<td>O(_2) *</td>
<td></td>
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<tr>
<td>Dichloroethene *</td>
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* High proportion of the total product use
Photolithography

- Photoresist Coating Processes
- Exposure Processes
Photolithography – Alignment & exposure

- Shutter is closed during focus and alignment and removed during wafer exposure.
- Reticle (may contain one or more die in the reticle field).
- Projection lens (reduces the size of reticle field for presentation to the wafer surface).
- Single field exposure, includes: focus, align, expose, step, and repeat process.

Wafer stage controls position of wafer in X, Y, Z, θ.)
Lithography Pattern Preparation

- Reticle
- Chrome Pattern
- Pellicle
- Quartz Substrate
Modern photolithography is based on optical lithography, which consists of an ultraviolet light source, optical system, a reticle with a die pattern, an alignment system, and a wafer covered with a light-sensitive photoresist.

Equipment called wafer steppers and step-and-scan systems have three basic purposes: 1) focus and align the wafer to the reticle, 2) reproduce a reticle image on the wafer through exposure of the resist, and 3) meet wafer throughput objectives. A general trend is the shorter the wavelength of the exposing light, the better resolution of the feature.

Optical Lithography

- An ultraviolet (UV) light source is required for optical lithography. Traditionally, this has been a mercury arc lamp at different wavelength intensity peaks (g-line of 436 nm, h-line at 405 nm and i-line at 365 nm). An excimer laser light source is used at UV wavelengths of 248 nm and below to achieve more light intensity. The laser sources used are krypton-fluoride (KrF) at a wavelength of 248 nm, argon-fluoride (ArF) at 193 nm and fluorine (F2) at 157 nm.

- Optics is important because photolithography is based on an optical imaging process. Reflection and refraction of light are used in optics. Many different types of lenses are used in optics. Lens material is traditionally glass, with fused silica used in some 248 nm applications and calcium fluoride (CaF2) used for shorter UV wavelengths (e.g., 193 nm and below).

- Diffraction is the bending of light as it passes through narrow openings, and is a concern in photolithography because of the small patterns on the reticle. Numerical aperture (NA) is the ability of a lens to collect and image diffracted light by converging the diffracted light to a single point. A larger NA is desirable.

- Antireflective coatings are used to reduce reflectivity from the surface below the resist. This controls problems from reflective notching and standing waves.

- The formula for resolution (R) is: \( R = \frac{k \lambda}{NA} \). If the wavelength (\( \lambda \)) is decreased, then the resolution of the system will decrease (which is desirable). If NA is increased (to collect more diffracted light), then resolution will also decrease.
Photolithography equipment history

• The contact aligner was the first alignment system. It used a 1X mask and is not widely used today. The proximity aligner was an improvement over the contact aligner because the mask did not contact the wafer. The latter is still used in low-volume laboratory applications.

• The scanning projection aligner (scanner) was developed in the late 1970s, and projects a full mask onto the wafer surface using a mirror system. It is still used today in older fabs with linewidths greater than 1 micron.

• The step-and-repeat aligner (stepper) was the mainstay of optical lithography in the 1990s. It is still widely used for CDs down to 0.35 μm. It projects one exposure field on the wafer and then steps to the next wafer location to repeat the exposure.

• The step-and-scan system is a hybrid tool that uses a scan approach (taken from the scanning projection aligner) along with a reduction lens and 4X reticle to step to exposure fields on the wafer surface. The scanning system has a simpler lens design.

• Reticles are a transparent plate that has the image pattern for an exposure field. They are used in steppers and step-and-scan systems. Reticles have a reduction ratio (typically 5:1 or 4:1) to permit a larger reticle pattern than what is imaged on the wafer. Reticles are fabricated with electron-beam lithography. A transparent pellicle is placed on the surface of the reticle to protect its surface from contamination.

• An important optical enhancement technique is phase-shift mask, which overcomes light diffraction problems. Other enhancement techniques are optical proximity correction, off-axis illumination and print bias.

• A wide range of alignment marks and systems are used to ensure the wafer is properly aligned to the reticle.
Applying Photo Resist –
scale: wafer level (~300mm / 12 inch)
The liquid (blue here) that’s poured onto the wafer while it spins is a photo resist finish similar as the one known from film photography. The wafer spins during this step to allow very thin and even application of this photo resist layer.

Exposure –
scale: wafer level (~300mm / 12 inch)
The photo resist finish is exposed to ultra violet (UV) light. The chemical reaction triggered by that process step is similar to what happens to film material in a film camera the moment you press the shutter button. The photo resist finish that’s exposed to UV light will become soluble. The exposure is done using masks that act like stencils in this process step. When used with UV light, masks create the various circuit patterns on each layer of the microprocessor. A lens (middle) reduces the mask’s image. So what gets printed on the wafer is typically four times smaller linearly than the mask’s pattern.

Exposure –
scale: transistor level (~50-200nm)
Although usually hundreds of microprocessors are built on a single wafer, this picture story will only focus on a small piece of a microprocessor from now on – on a transistor or parts thereof. A transistor acts as a switch, controlling the flow of electrical current in a computer chip. Intel researchers have developed transistors so small that about 30 million of them could fit on the head of a pin.
Photoresist Coating Processes

Photoresists
- Negative Photoresist *
- Positive Photoresist *

Other Ancillary Materials (Liquids)
- Edge Bead Removers *
- Anti-Reflective Coatings *
- Adhesion Promoters/Primers (HMDS) *
- Rinsers/Thinners/Corrosion Inhibitors *
- Contrast Enhancement Materials *

Developers
- TMAH *
- Specialty Developers *

Inert Gases
- Ar
- N₂
Exposure Processes

Expose
  Kr + F₂ (gas) *

Inert Gases
  N₂
Ion Implantation

- Well Implants
- Channel Implants
- Source/Drain Implants
Ion Implantation

Process Conditions
Flow Rate: 5 sccm
Pressure: 10^-5 Torr
Accelerating Voltage: 5 to 200 keV

Gases
- Ar
- AsH₃
- B₁¹F₃ *
- He
- N₂
- PH₃
- SiH₄
- SiF₄
- GeH₄

Solids
- Ga
- In
- Sb

Liquids
- Al(CH₃)₃

* High proportion of the total product use
Implanted Ion Path

Typical Values

- Deep Retrograde Well = 800-1000 KcV or 1-3 x 10^{13} ions/cm^3
- N-Well = 200 KcV or 1 x 10^{13} ions/cm^3
- Source-Drain = 30 KcV or 3-5 x 10^{15} ions/cm^3
- Buried Layer = 80-100 KcV or 1-5 x 10^{15} ions/cm^3
- Resistors = 50 KcV or .1-10 x 10^{13} ions/cm^3
**Applying Photo Resist** – scale: transistor level (~50-200nm)
There’s photo resist (blue color) applied, exposed and exposed photo resist is being washed off before the next step. The photo resist will protect material that should not get ions implanted.

**Ion Implantation** – scale: transistor level (~50-200nm)
Through a process called ion implantation (one form of a process called doping), the exposed areas of the silicon wafer are bombarded with various chemical impurities called ions. Ions are implanted in the silicon wafer to alter the way silicon in these areas conducts electricity. Ions are shot onto the surface of the wafer at very high speed. An electrical field accelerates the ions to a speed of over 300,000 km/h (~185,000 mph).

**Removing Photo Resist** – scale: transistor level (~50-200nm)
After the ion implantation the photo resist will be removed and the material that should have been doped (green) has alien atoms implanted now (notice slight variations in color).
Etch

• Conductor Etch
  - Poly Etch and Silicon Trench Etch
  - Metal Etch
• Dielectric Etch
Etching Terminology

• Isotropic Etching – Etching which is not directional. The etchant etches down and sideways at the same rate. Most wet etches are Isotropic.

• Anisotropic Etching – Etching which proceeds faster in one direction than in other directions, i.e., a directional etch. Some plasma and ion beam etches are directional.

• Selectivity – The relative etch rate for an etchant for one material versus another material. For example, hydrofluoric acid etches oxide but not silicon; hydrofluoric acid, therefore, has a high selectivity for oxide over silicon.
Etching

**Washing off of Photo Resist**
*scale: transistor level (~50-200nm)*
The gooey photo resist is completely dissolved by a solvent. This reveals a pattern of photo resist made by the mask.

**Etching**
*scale: transistor level (~50-200nm)*
The photo resist is protecting material that should not be etched away. Revealed material will be etched away with chemicals.

**Removing Photo Resist**
*scale: transistor level (~50-200nm)*
After the etching the photo resist is removed and the desired shape becomes visible.

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Sand / Ingot

Sand
With about 25% (mass) Silicon is the second most frequent chemical element in the earth's crust. Sand—especially Quartz—has high percentages of Silicon in the form of Silicon dioxide (SiO$_2$) and is the base ingredient for semiconductor manufacturing.

Melted Silicon
*scale: wafer level (~300mm/12 inch)*
Silicon is purified in multiple steps to finally reach semiconductor manufacturing quality which is called Electronic Grade Silicon. Electronic Grade Silicon may only have one alien atom every one billion Silicon atoms. In this picture you can see how one big crystal is grown from the purified silicon melt. The resulting mono crystal is called Ingot.
Isotropic Versus Anisotropic Etching

Isotropic Etch

Anisotropic Etch

Partial Etch

Etch Complete

Over Etch
Anisotropic Etch Mechanisms

Ion bombardment creates a surface damage layer.

Chemical etchants - etch away the damage layer, ion bombardment creates a new damage layer.

Inhibitor covers the whole surface inhibiting etching.

Ion bombardment removes the inhibitor from the bottom of the exposed area.

Chemical etchants - etch the area where the inhibitor has been removed by ion bombardment.

Inhibitor
• Critical Cleaning
• Photoresist Strips
• Pre-Deposition Cleans
Critical Cleaning

Process Conditions
Temperature: Piranha Strip is 180 degrees C.

1 Organics
H₂SO₄ + H₂O₂
H₂O Rinse

2 Oxides
HF + H₂O
H₂O Rinse

3 Particles
NH₄OH + H₂O₂ + H₂O
H₂O Rinse

4 Metals
HCl + H₂O₂ + H₂O
H₂O Rinse

5 Dry
H₂O or IPA + N₂

RCA Clean
SC1 Clean (H₂O + NH₄OH + H₂O₂) *
* SC2 Clean (H₂O + HCl + H₂O₂) *

Piranha Strip
* H₂SO₄ + H₂O₂ *

Nitride Strip
H₃PO₄ *

Oxide Strip
HF + H₂O *

Dry Strip
N₂O
O₂
CF₄ + O₂
O₃

Solvent Cleans
NMP
Proprietary Amines (liquid)

Dry Cleans
HF
O₂ Plasma
Alcohol + O₃
Chamber Cleaning

Chemical Reactions
Oxide Etch: \( \text{SiO}_2 + \text{C}_2\text{F}_6 \rightarrow \text{SiF}_4 + \text{CO}_2 + \text{CF}_4 + 2 \text{CO} \)

Process Conditions
Flow Rates: 10 to 300 sccm
Pressure: 10 to 100 mTorr
RF Power: 100 to 200 Watts

Chamber Cleaning
- \( \text{C}_2\text{F}_6 \) *
- \( \text{NF}_3 \)
- \( \text{ClF}_3 \)

* High proportion of the total product use
Planarization

- Electroplating
- Oxide planarization
- Metal Planarization
Metal Deposition

**Ready Transistor** –
*scale: transistor level (~50-200nm)*
This transistor is close to being finished. Three holes have been etched into the insulation layer (magenta color) above the transistor. These three holes will be filled with copper which will make up the connections to other transistors.

**Electroplating** –
*scale: transistor level (~50-200nm)*
The wafers are put into a copper sulphate solution as this stage. The copper ions are deposited onto the transistor thru a process called electroplating. The copper ions travel from the positive terminal (anode) to the negative terminal (cathode) which is represented by the wafer.

**After Electroplating** –
*scale: transistor level (~50-200nm)*
On the wafer surface the copper ions settle as a thin layer of copper.
Metal Layers

Polishing - scale: transistor level (~50-200nm)
The excess material is polished off.

Metal Layers - scale: transistor level (six transistors combined ~500nm)
Multiple metal layers are created to interconnect (think: wires) in between the various transistors. How these connections have to be "wired" is determined by the architecture and design teams that develop the functionality of the respective processor (e.g. Intel® Core™ i7 Processor). While computer chips look extremely flat, they may actually have over 20 layers to form complex circuitry. If you look at a magnified view of a chip, you will see an intricate network of circuit lines and transistors that look like a futuristic, multi-layered highway system.
Chemical Mechanical Planarization (CMP)

Process Conditions (Oxide)
Flow: 250 to 1000 ml/min
Particle Size: 100 to 250 nm
Concentration: 10 to 15%, 10.5 to 11.3 pH

Process Conditions (Metal)
Flow: 50 to 100 ml/min
Particle Size: 180 to 280 nm
Concentration: 3 to 7%, 4.1 - 4.4 pH

Backing (Carrier) Film
Polyurethane

Pad
Polyurethane

Pad Conditioner
Abrasive

CMP (Oxide)
Silica Slurry *
KOH *
NH₄OH
H₂O

CMP (Metal)
Alumina *
FeNO₃

* High proportion of the total product use.
Metallization

Traditional Interconnect Flow

1. Cap ILD layer and CMP
2. Oxide Via-2 etch
3. Tungsten deposition + CMP
4. Metal-2 deposition + etch

Dual Damascene Flow

1. Cap ILD layer and CMP
2. Nitride etch-stop layer (patterned and etched)
3. Second ILD layer deposition and etch through two oxide layers
4. Copper fill
5. Copper CMP
Metallization

• Wafer metallization is the deposition of a thin film of conductive metal onto the wafer surface.

• There is traditional (aluminum) metallization and the new dual damascene (copper) metallization.

Types of Metals

• Metals and metal alloys used in wafer fabrication are: aluminum, aluminum-copper alloys, copper, barrier metals, silicides and metal plugs. Aluminum is the traditional interconnect metal. Aluminum-copper alloys are used to reduce electromigration.

• Copper metallization is deposited using a dual damascene approach that is based on etching trenches and vias into the dielectric, filling the trenches and vias with copper and then planarizing the copper with chemical mechanical planarization. Copper is the ideal interconnect metal. Its benefits are: 1) reduction in resistivity, 2) reduction in power consumption, 3) tighter packing density, 4) superior resistance to electromigration and 5) fewer process steps.

• A barrier metal is a thin layer of deposited metal that prevents intermixing of the materials above and below the barrier.

• Refractory metals react with silicon to form a silicide. A silicide is a metal compound that is thermally stable and has low electrical resistivity at the silicon/refractory metal interface. A salicide structure (self-aligned silicide) attains properly aligned source, drain and polysilicon gate in transistors.

• Metal plugs fill the via connections between two conductive layers.
Example CMOS process flow
0.25 μm CMOS Process Flow 1

1. Clean Wafers
2. Grow Thin Stress Relief Oxide
3. Deposit LPCVD Nitride
4. N Tub Photo – Mask 1
5. RIE Etch Nitride
6. Phosphorus Implant – Forms N Tub
7. Strip Resist
8. Clean Wafers
9. Deposit Thick Oxide
0.25 µm CMOS Process Flow 2

10. CMP Oxide Down to Nitride
11. Post CMP Clean
12. Wet Strip Nitride
13. Clean Wafers
14. Boron Implant – Forms P Tub
15. Strip Oxide
16. Clean Wafers
17. Rapid Thermal Anneal Implants
0.25 µm CMOS Process Flow 3

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<td>Deposit LPCVD Nitride</td>
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0.25 µm CMOS Process Flow 4

30 Strip Resist
31 P+ Channel Stop Photo – Mask 4
32 P+ Channel Stop Implant

33 Strip Resist
34 Clean Wafers
35 Deposit Oxide

36 CMP Oxide Down to Nitride
0.25 µm CMOS Process Flow 5

- 37 Wet Strip Nitride
- 38 Strip Thin Oxide
- 39 Clean Wafers
- 40 Grow Thin Stress Relief Oxide
- 41 N Threshold Adjust Photo – Mask 5
- 42 N Threshold Adjust Implant
- 43 Strip Resist
- 44 P Threshold Adjust Photo – Mask 6
- 45 P Threshold Adjust Implant
0.25 μm CMOS Process Flow 6

- Strip Resist
- Clean Wafers
- Rapid Thermal Anneal Implants
- Strip Thin Oxide
- Clean Wafers
- Grow Gate Oxide
- Deposit Doped Polysilicon
- Deposit Tungsten Silicide
- Polysilicon Gate Photo – Mask 7
- RIE Etch Silicide and Polysilicon
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<tr>
<td>123</td>
<td>RIE Etch Oxide</td>
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</table>
Test and assembly:

- Wafer inspection

- Wafer probe / bumped wafer probe
  - 300mm wafer probe / bumped wafer probe
  - Vertical wafer / bumped wafer probe
  - Laser trim

- Final test

- Dry-bake, packing, tape and reel