Newer process technology (since 1999) includes:

- copper metalization
- hi-k dielectrics for gate insulators
- silicon on insulator
- strained silicon
- lo-k dielectrics for interconnects
- Immersion lithography for masks
- Extreme UV – EUV 13.5nm wavelength
Copper metallization

Copper could not be patterned by the previous techniques of photoresist masking and plasma etching that had been used with great success with aluminium since there were no volatile copper compounds available. This inability to plasma etch copper called for a new approach to the metal patterning process and the result of this rethinking was a process referred to as an additive patterning, also known as a "Damascene" or "dual-Damascene" process by analogy to a traditional technique of metal inlaying.

In this process, the underlying silicon oxide insulating layer is patterned with open trenches where the conductor should be. A thick coating of copper that significantly overfills the trenches is deposited on the insulator, and chemical-mechanical planarization (CMP) is used to remove the copper (known as overburden) that extends above the top of the insulating layer. Copper sunken within the trenches of the insulating layer is not removed and becomes the patterned conductor.

The first copper-based microprocessors

On September 1, 1998, IBM announced the shipment of the world’s first copper-based microprocessors. The IBM® PowerPC® 750 was originally created as a standard aluminum design operating at up to 300 MHz. By applying IBM’s copper manufacturing process to what was essentially the same chip, the company was able to produce semiconductors featuring speeds of at least 400 MHz—a 33 percent speed improvement for the same chip.
Research by Intel has shown that a thicker high-k dielectric gate increases overall capacitance while decreasing the leakage current by ~100X.

These new High-k materials are Hafnium-based and have $k > 3.9$, the dielectric constant of SiO2.
**si on insulator (SOI)**

- refers to the use of a layered silicon-insulator-silicon substrate in place of conventional silicon substrates in semiconductor manufacturing, especially microelectronics, to reduce parasitic device capacitance, thereby improving performance.

**Benefits**

- Lower parasitic capacitance due to isolation from the bulk silicon, which improves power consumption at matched performance.
- Resistance to latchup due to complete isolation of the n- and p-well structures.
- Higher performance at equivalent VDD. Can work at low VDD's.
- Reduced temperature dependency due to no doping.
- Better yield due to high density, better wafer utilization.
- Reduced antenna issues
- No body or well taps are needed.
- Lower leakage currents due to isolation thus higher power efficiency.
- Inherently radiation hardened (resistant to soft errors), thus reducing the need for redundancy.
**strained silicon**

- A layer of silicon in which the silicon atoms are stretched beyond their normal interatomic distance. This can be accomplished by putting the layer of silicon over a substrate of silicon germanium (SiGe).
- When silicon is deposited on top of a substrate with atoms spaced farther apart, the atoms in silicon stretch to line up with the atoms beneath, stretching -- or "straining" -- the silicon. In the strained silicon, electrons experience less resistance and flow up to 70 percent faster, which can lead to chips that are up to 35 percent faster -- without having to shrink the size of transistors.

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**High Stress Film**

- PMOS: ~30% drive current increase
- NMOS: ~10% drive current increase
**lo-k dielectrics for interconnects**

- A low-κ dielectric is a material with a small dielectric constant relative to silicon dioxide.
- Replacing the silicon dioxide with a low-κ dielectric of the same thickness reduces parasitic capacitance, enabling faster switching speeds and lower heat dissipation.

- New low-k carbon doped oxide (CDO) used for interconnect dielectric
- CDO provides ~20% capacitance reduction compared to SiO₂
- Reduced interconnect capacitance provides improved performance and lower chip power
Immersion lithography for masks

- A photolithography resolution enhancement technique for manufacturing integrated circuits (ICs) that replaces the usual air gap between the final lens and the wafer surface with a liquid medium that has a refractive index greater than one. The resolution is increased by a factor equal to the refractive index of the liquid. Current immersion lithography tools use highly purified water for this liquid, achieving feature sizes below 45 nanometers.

In immersion lithography, light travels down through a system of lenses and then a pool of water before reaching the photoresist on top of the wafer.
# Intel Technology Roadmap

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<th>Process Name</th>
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<td>45 nm</td>
<td>32 nm</td>
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<td>14 nm</td>
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<td>1&lt;sup&gt;st&lt;/sup&gt; Production</td>
<td>2007</td>
<td>2009</td>
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Intel continues our cadence of introducing a new technology generation every two years.
Traditional Planar Transistor

Traditional 2-D planar transistors form a conducting channel in the silicon region under the gate electrode when in the “on” state.
3-D Tri-Gate transistors form conducting channels on three sides of a vertical fin structure, providing “fully depleted” operation.

*Transistors have now entered the third dimension!*
Tri-Gate transistors can have multiple fins connected together to increase total drive strength for higher performance
22 nm Tri-Gate Transistor

Tri-Gate transistors can have multiple fins connected together to increase total drive strength for higher performance
22 nm Tri-Gate Transistor
Silicon substrate voltage exerts some electrical influence on the inversion layer (where source-drain current flows). The influence of substrate voltage degrades electrical sub-threshold slope (transistor turn-off characteristics) NOT fully depleted.
Std vs. Fully Depleted Transistors

Partially Depleted SOI (PDSOI)

“Transistor 101”

Floating body voltage exerts some electrical influence on the inversion layer, degrading sub-threshold slope
NOT fully depleted
Not used by Intel
Std vs. Fully Depleted Transistors

Fully Depleted SOI (FDSOI)

“Transistor 101”

Floating body eliminated and sub-threshold slope improved
Requires expensive extremely-thin SOI wafer, which adds ~10% to total process cost
Not used by Intel
Std vs. Fully Depleted Transistors

Fully Depleted Tri-Gate Transistor

Gate electrode controls silicon fin from three sides providing improved sub-threshold slope
Inversion layer area increased for higher drive current
Process cost adder is only 2-3%
Transistor Operation

Transistor current-voltage characteristics
The “fully depleted” characteristics of Tri-Gate transistors provide a steeper sub-threshold slope that reduces leakage current.
Transistor Operation

The steeper sub-threshold slope can also be used to target a lower threshold voltage, allowing the transistors to operate at lower voltage to reduce power and/or improve switching speed.
Transistor Gate Delay

“Transistor 101”

Transistor Gate Delay (normalized)

Transistor gate delay (switching speed) slows down as operating voltage is reduced
Transistor Gate Delay

22 nm planar transistors could provide some performance improvement, but would still have poor gate delay at low voltage
22 nm Tri-Gate transistors provide improved performance at high voltage and an *unprecedented* performance gain at low voltage
22 nm Tri-Gate transistors can operate at lower voltage with good performance, reducing active power by >50%.

Transistor Gate Delay

Transistor Gate Delay (normalized)
Tri-Gate Transistor Benefits

- Dramatic performance gain at low operating voltage, better than Bulk, PDSOI or FDSOI
  - 37% performance increase at low voltage
  - >50% power reduction at constant performance
- Improved switching characteristics (On current vs. Off current)
- Higher drive current for a given transistor footprint
- Only 2-3% cost adder (vs. ~10% for FDSOI)

Tri-Gate transistors are an important innovation needed to continue Moore’s Law
22 nm Tri-Gate Circuits

- 364 Mbit array size
- >2.9 billion transistors
- 3rd generation high-k + metal gate transistors
- Same transistor and interconnect features as on 22 nm CPUs

22 nm SRAMs using Tri-Gate transistors were first demonstrated in Sept. „09

Intel is now demonstrating the world’s first 22 nm microprocessor (Ivy Bridge) and it uses revolutionary Tri-Gate transistors

22 nm SRAM, Sept. „09
EUV Lithography

Modern semiconductor production tools use deep ultraviolet (DUV) argon fluoride (ArF) excimer lasers with 193 nm wavelength.

One of the key transistor density improving technologies is immersion lithography, which replaces the air gap between the lens and wafer with liquid, whose refraction index is higher than one. For example, purified deionized water has refraction index of 1.44 and this allows to enhance resolution of production tools by up to 40% depending on materials.

Another key tech for contemporary semiconductor manufacturing is called multiple patterning, a semiconductor production technique that allows to increase feature density by resolving multiple lines on the same photoresist layer using multiple photomasks. Usage of multi-patterning essentially means that certain layers within one chip are exposed multiple times, which greatly increases complexity of manufacturing operations and stretches production cycles, essentially increasing costs of chips.
EUV lithography, whose development started in 1985 and which used to be called Soft X-Ray, utilizes extreme ultraviolet wavelength of 13.5 nm.

TSMC can produce 46 nm metal pitches with a single exposure, an operation that requires usage of four masks for an ArF scanner. Moreover, Intel has managed to produce wafers with 22 nm metal pitches using its own micro EUV tool. Among other advantages, EUV is expected to shrink cycle times and promises to increase yields of chips at advanced nodes. Unfortunately, EUV is an extremely complex technology that not only requires all-new step-and-scan systems for production of semiconductors, new chemicals and new mask infrastructure, but it is also so tricky to use that its actual resolution can end up far below expectations.
EUV Lithography

It should be noted that generation of EUV light is a rather difficult process itself. Cymer, a division of ASML that produces light sources for lithography tools, is developing laser produced plasma (LPP) EUV sources. The LPP technology applies CO$_2$ laser to small tin droplets (which are around 30 microns in diameter), creating ionized gas plasma at electron temperatures of several tens of electron volts. The 13.5 nm radiation is then collected by a special ~0.5 meter mirror coated with several layers of molybdenum (Mo) and silicon (Si), in order to selectively reflect the maximum possible amount of 13.5 nm EUV light and direct it to the Intermediate Focus (IF) position at the entrance to the scanner system.
To put it simply: in order to generate 13.5 nm EUV light in a special **plasma chamber**, you need a very powerful laser (because a significant amount of its power will be wasted); a generator and a catcher for tin droplets (in addition to a debris collector); as well as a special, nearly perfect, elliptical mirror. To make everything even trickier, since EUV light with 13.5 nm wavelength can be absorbed by almost any matter, EUV lithography has to be done in vacuum. This also means that traditional lenses cannot be used with EUV because they absorb 13.5 nm light; instead, specialized multilayer mirrors are used. Even such mirrors absorb about 30% of the light, which is why powerful light sources are needed. This level of absorption can lead to ablative effects on the mirrors themselves, which introduces additional engineering challenges.
The 13.5 nm EUV light generator needs to have a powerful light source that can expose economically viable amount of wafers per hour (or day). One of the key issues with the TWINCSCAN NXE scanners was that is their laser produced plasma EUV source was not powerful enough. Until recently, performance of experimental EUV equipment from ASML, such as the TWINCSCAN NXE:3300B scanners, was limited to around 500 wafers per day due to power source limitations. By contrast, the current-generation TWINSCAN NXT scanners can process from 175 to 275 wafers per hour (which is good enough, considering heavy usage of multi-patterning). The reliability of the droplet generator was mediocre just about a year ago. Moreover, lifetime of the collector mirror is a yet another point of concern due to the previously mentioned ablative effects.
Finally, while step-and-scan systems with EUV's 13.5 nm wavelength will help to produce microprocessors and other chips using 5 nm and, perhaps, 7nm, technologies, contemporary 193nm ArF tools are not going anywhere. Virtually all chipmakers say that EUV scanners will only be used for critical layers of chips. For layers that can be produced using multi-patterning, DUV tools will be used.