Assembly and Packaging

Introduction

Chips that pass the wafer sort test undergo final assembly and packaging. IC final assembly separates each good die from the wafer and attaches the die to a metal leadframe or substrate. IC packaging encloses the die in a protective package.

IC packaging has four functions: protection from the environment/handling, signal interconnections, physical support and heat dissipation. There are two packaging levels: 1st level packaging involves the IC, whereas 2nd level packaging is placing the IC on a circuit board. There are numerous packaging design constraints.

Traditional Assembly

IC final assembly consists of four steps: backgrind, die separation, die attach and wire bonding. Backgrind reduces the wafer thickness to the appropriate dimension. Die separation cuts each die from the wafer. Die attach is the physical attachment of the die to the leadframe or substrate. Wirebonding attaches fine-diameter wires between die bonding pads and the terminals of the leadframe to form electrical connections.

Die attach is done by epoxy attach, eutectic attach and glass frit attach. The common epoxy attach method bonds the chip to the leadframe using epoxy. Eutectic attach, Quad flat pack (QFP), Leadless chip carrier (LCC), Plastic leaded chip carrier (PLCC), Thin small outline package (TSOP), Dual in-line package (DIP), Single in-line package (SIP), Single in-line package (SIP), Thin small outline package (TSOP), Quad flat pack (QFP), Plastic leaded chip carrier (PLCC), Leadless chip carrier (LCC)
• Chips that pass the wafer sort test undergo final assembly and packaging. IC final assembly separates each good die from the wafer and attaches the die to a metal leadframe or substrate. IC packaging encloses the die in a protective package.

• IC packaging performs four functions: protection from the environment/handling, signal interconnections, physical support and heat dissipation. There are two packaging levels:
- 1st level packaging involves the IC
- 2nd level packaging places the IC on a circuit board.

There are numerous packaging design constraints.
IC final assembly consists of four steps:

Backgrind - reduces the wafer thickness to the appropriate dimension.

die separation - cuts each die from the wafer.

die attach - the physical attachment of the die to the leadframe or substrate. Die attach is done by epoxy attach, eutectic attach and glass frit attach.

wire bonding - attaches fine-diameter wires between die bonding pads and the terminals of the leadframe to form electrical connections. The three basic types of wirebonding are: thermocompression bonding, ultrasonic bonding and thermosonic ball bonding.
• Traditional IC packaging materials are plastic packaging and ceramic packaging.

• Plastic packaging uses an epoxy polymer to encapsulate the wirebonded die and leadframe. This technology has many different types of plastic packages.

• Ceramic packaging is used for state-of-the-art IC packages that require either maximum reliability or high-power. The two main types of ceramic packaging are either a refractory (high temperature) ceramic or ceramic DIP (CERDIP) technology. Both have a hermetic seal (sealed against moisture).

• All assembled and packaged chips undergo a final electrical test for IC reliability.
Advanced packaging designs include:

**Flip chip** - mounts the active side of a chip toward the substrate. It uses bump technology (typically solder bumps) to form the interconnection between the chip and substrate. An epoxy underfill is used around the area-array of bumps to improve reliability.

**Ball grid array (BGA)** - uses a ceramic or plastic substrate with an area array of solder balls to connect the substrate to the circuit board. To lower costs, this technology is readily integrated into standard surface mount assembly.

**Land Grid Array (LGA)** - is a packaging technology with a square grid of contacts on the underside of a package. The contacts are to be connected to a grid of pin contacts on the PCB.

**Chip on board (COB)** - mounts IC chips directly to the substrate, along side other surface mount (SMT) or pin-in-hole (PIH) components.

**Tape automated bonding (TAB)** - uses a plastic tape as a chip carrier. The tape has a thin copper foil that is etched to form the leads. The chip and leads are removed from the carrier prior to assembly onto the circuit board.

**Multichip modules (MCM)** - has several die assembled onto one substrate. This permits a higher density of chips.

**Chip scale packaging (CSP)** - an IC package that is about the same size as the silicon chip (< 1.2 times the footprint of the die). This is a fast growing method of advanced packaging, and provides for lower cost, lower weight and lower thickness.

**Wafer-level packaging** - places the 1st level interconnections and package input/output terminals on the wafer before it is diced. It is typically done with a bump interconnect process. This will simplify the IC packaging process and lower cost.