Basic Computer operations
First step - Booting Sequence

- BIOS starts
  - checks how much RAM
  - keyboard
  - other basic devices
- PnP (Plug-And-Play) initialized
- BIOS determines boot Device
  - By reading the Master Boot Record (MBR)
- The first sector in boot device is read into memory and executed to determine active partition
  - This first sector contains the boot loader.
- Secondary boot loader is loaded from that partition.
- This loader loads the OS from the active partition and starts it.
The fundamental purpose of the Basic Input Output System (BIOS) is to initialize and test the system hardware components, and to load a bootloader or an operating system from a mass memory device. The BIOS also provides an abstraction layer for the hardware.

The Unified Extensible Firmware Interface (UEFI) is a specification that defines a software interface between an operating system and platform firmware. UEFI is meant to replace the Basic Input/Output System (BIOS) firmware interface, present in all IBM PC-compatible personal computers.
For PnP to work properly the system needs:

- **PnP BIOS**: reads Extended System Configuration Data (ESCD), which is a file that contains information about installed PnP devices.
- **PnP OS**
- **PnP enabled device** (almost all devices these days are like that).
BIOS and PnP

Example: we connect a sound card to the PCI bus:

1. The BIOS initiates the PnP BIOS.
2. The PnP BIOS scans the PCI bus for hardware by sending out a signal to any device connected to the bus, asking the device who it is.
3. The sound card responds by identifying itself. The device ID is sent back across the bus to the BIOS.
4. The PnP BIOS checks the ESCD to see if the configuration data for the sound card is already present.
   5. The PnP BIOS assigns IRQ, DMA, memory address and I/O settings to the sound card and saves the data in the ESCD.
   6. When the OS boots, it will read the info in ESCD and install required driver.
Model Computer System
Anatomy of A Motherboard

- **Chipset**: handles communication between the processor and the other parts of your computer.
- **CPU slot** (socket)
- **Buses**: connection on the motherboard that carries data between the various parts of the motherboard (chipset, memory, processor, ...)
- **Expansion slots**: for connecting expansion cards
- **Memory slots**
- **Power connector**: to supply power to motherboard and to help motherboard supply power to some devices
- **Others**: like graphics and sound (integrated)
- **Clock generator**
Chipset

• Designed for use with a specific family of processors.
• **Northbridge**: connects the CPU to high-speed components like RAM.
• **Southbridge**: connects to slower peripheral devices like PCI slots, USB, IDE, … .
• Example: Intel southbridge connects to northbridge with 266MB/s. Other chipsets are faster.
• Both bridges are essentially routers. They route data traffic from one bus to another.
Chipset

South Bridge

North Bridge

source: http://static.ddmcdn.com/gif/motherboard-bridges.jpg
Bus/Bridge Chipset

Traditional North/South bridge chips

Intel x79 Chipset architecture

PCI Express* 2.0 Graphics
- Support for multi-card configurations
  - 2x16 & 1x8
  - 1x16 & 3x8 or
  - 1x16 & 2x8 2x4

2nd Gen Intel® Core™ i7 Processors
- LGA 2011

DDR3 memory 12.8 GB/s
- Intel® High Definition Audio
- 14 Hi-Speed USB 2.0 Ports; Dual EHCI; USB Port Disable
- Intel® Integrated 10/100/1000 MAC
- Intel® Gigabit LAN Connect
- Intel® ME Firmware and BIOS Support
- Intel® Extreme Tuning Support
- Intel® Rapid Storage Technology enterprise 3.0
- DMI 20 Gb/s
- 8 PCI Express* 2.0
- 6 Serial ATA Ports: eSATA; Port Disable

1 Theoretical maximum bandwidth
2 All SATA ports capable of 3 Gb/s, 2 ports capable of 6 Gb/s.

Intel® X79 Express Chipset Block Diagram
Model Computer System

- Pentium 4 Processor
- System bus (800 MHz, 604 GB/sec)
- AGP 8X (2.1 GB/sec)
- Graphics output
- Memory controller hub (north bridge) 82875P
- DDR 400 (3.2 GB/sec)
- Main memory DIMMs
- Serial ATA (150 MB/sec)
- Disk
- Parallel ATA (100 MB/sec)
- CD/DVD
- Tape
- I/O controller hub (south bridge) 82801EB
- Parallel ATA (100 MB/sec)
- AC/97 (1 MB/sec)
- Stereo (surround sound)
- USB 2.0 (60 MB/sec)
- 1 Gbit Ethernet
- PCI bus (132 MB/sec)
- 10/100 Mbit Ethernet
Ex.: Asus RAMPAGE IV EXTREME Motherboard
Modern (2014) Motherboard Specifications

CPU
Intel® Socket 2011 for 2nd Generation Core™ i7 Processors
Supports Intel® Turbo Boost Technology 2

Chipset
Intel® X79

Memory
8 x DIMM, Max. 64GB, DDR3 2400(O.C.)/2133(O.C.)/
1866/1600/1333/1066 MHz Non-ECC, Un-buffered Memory
Quad Channel Memory Architecture
Supports Intel® Extreme Memory Profile (XMP)

Multi-GPU Support
Supports NVIDIA® 4-Way SLI™ Technology
Supports AMD 4-Way CrossFireX Technology

Expansion Slots
4 x PCIe 3.0/2.0 x16 (x16 or dual x16 or x16/x8/x16 or x16/
x8/x8/x8, red) *1
1 x PCIe 3.0/2.0 x16 (x8 mode, gray) *1
1 x PCIe 2.0 x1

Storage
Intel® X79 chipset :
2 x SATA 6Gb/s port(s), red
4 x SATA 3Gb/s port(s), black
Support Raid 0, 1, 5, 10
ASMedia® PCIe SATA controller :
2 x eSATA 6Gb/s port(s), red
2 x SATA 6Gb/s port(s), red

LAN
Intel®, 1 x Gigabit LAN Controller(s)
Bluetooth
Bluetooth V2.1+EDR

Audio
Realtek® ALC898 7.1-Channel High Definition Audio CODEC
- Supports : Jack-detection, Multi-streaming, Front Panel Jack-retasking
Audio Feature :
- Blu-ray audio layer Content Protection
- Optical S/PDIF out port(s) at back panel

USB Ports
ASMedia® USB 3.0 controller :
8 x USB 3.0 port(s) (4 at back panel, blue, 4 at mid-board)
Intel® X79 chipset :
12 x USB 2.0 port(s) (8 at back panel, black+red, 4 at mid-board)

Power:
- 8 -phase CPU power design
- 3 -phase VCCSA power design
2 + 2 phase DRAM power design

Overclocking Protection :
- COP EX (Component Overheat Protection - EX)
Voltminder LED II
Modern (2014) Motherboard features

LGA2011 Intel® Core™ i7

This motherboard supports the latest Intel® Sandy Bridge-E processors in the LGA2011 package, with memory and PCI Express controllers integrated to support 4-channel (8 DIMM) DDR3 memory and 16 PCI Express 3.0 lanes. This provides great graphics performance. Intel® Sandy Bridge-E processors are among the most powerful and energy efficient CPUs in the world.

Intel® X79 Chipset

The Intel® X79 Express Chipset is the latest single-chipset design that supports the new socket 2011 Intel® Core™ i7 Extreme Edition processors. It improves performance by utilizing serial point-to-point links, allowing for increased bandwidth and stability. Additionally, the X79 comes with 2 SATA 6Gb/s and 4 SATA 3Gb/s ports for faster data retrieval, doubling the bandwidth of current bus systems.

PCle 3.0 Ready

The latest PCI Express bus standard delivers improved encoding for twice the performance of current PCIe 2.0. Total bandwidth for a x16 link reaches a maximum of 32GB/s, double the 16GB/s of PCIe 2.0 (in x16 mode). PCIe 3.0 provides users unprecedented data speeds combined with the convenience and seamless transition offered by complete backward compatibility with PCIe1.0 and PCIe 2.0 devices. It is a must-have feature PC users aiming to improve and optimize graphics performance, as well as have the latest, most future-proof technology.
Buses

• To ensure interoperability of different devices with different buses, there must be well-defined rules about how the bus works, and which all attached devices must obey. 

    bus protocol

• A bus has address, data, and control lines.

• There is not necessarily a one-to-one mapping between CPU pins and bus lines.
  • A decoder chip between CPU and bus would be needed in this case.

• A synchronous bus has a line driven by a crystal oscillator.
  – The signal on this line consists of a square wave
  – All bus activities take an integral number of these cycles, called bus cycles.

• The asynchronous bus does not have a master clock.
  – Handshaking
Bus Type signals

asynchronous
(peripheral bus)

ReadReq
Data
Ack
DataRdy

synchronous
(system bus)

Clock
Read
Data
Disadvantage of Synchronous Buses

• Everything works in multiples of the bus clock.
  – Example: if a CPU and memory can complete a transfer in 3.1 cycles they have to stretch it to 4.0 because fractional cycles are forbidden.

• Once a bus cycle has been chosen, and memory and I/O cards have been built for it, it is difficult to take advantage of future improvements in technology.

• The bus has to be geared to the slowest devices on the bus.
I/O Schemes

Memory-mapped I/O
   Controlled by CPU
   I/O devices act as segments of memory
   CPU reads and writes “registers” on the I/O device
   Example: status register (done, error), data register

DMA (Direct Memory Access)
   Controlled by I/O device
   DMA controller transfers data directly between I/O device and memory
      DMA controller can become a bus master
      DMA controller is initialized by the processor and I/O device

Polling
   The processor periodically checks status bit to see if it is time for the next I/O operation.

Interrupts
   I/O device forces the CPU into the operating system to service an I/O device request
   Interrupts have priority (for simultaneous interrupts and preemption)
Interfacing I/O Devices to the Memory, Processor and Operating System

Three characteristics of I/O systems:

- *shared by multiple programs using the processor.*
- *often use interrupts to communicate information about I/O operations.*
- *The low-level control of an I/O device is complex.*

Three types of communication are required:

- *The OS must be able to give commands to the I/O device.*
- *The device must be able to notify the OS, when I/O device completed an operation or has encountered an error.*
- *Data must be transferred between memory and an I/O device.*
Giving Commands to I/O Devices

Methods used to address the device

**memory-mapped I/O:**
portions of the memory address space are assigned to I/O devices, and lw and sw instructions can be used to access the I/O port.

**special I/O instructions**
ex: in al, port out port, al

**command port ,data port**
The Status register (a done bit, an error bit......)
The Data register, The command register
Comparison of I/O transfer methods

The disadvantage of polling is that it wastes a lot of processor time.

- When the CPU polls the I/O devices periodically, the I/O devices might not have any requests or are not yet ready.

- If the I/O operations is interrupt driven, the OS can work on other tasks while data is being read from or written to the device.

- Because DMA doesn’t need the control of the processor, it will not consume much of processor time.

- This is the optimum approach if it can be used for the application.
DMA transfer - details

1. CPU programs the DMA controller by setting its registers so it knows what to transfer where.

2. The DMA controller initiates the transfer by issuing a read request to the disk controller.

3. The disk controller fetches the next word from its internal buffer and writes it to the memory.

4. When the write is finished, the disk controller sends an acknowledgement to the DMA controller.

5. If there are more data to transfer (counter is greater than 0), then the DMA controller repeats steps 2 through 4. If all the data has been transferred, the DMA controller interrupts the CPU to let it know that the transfer is complete.
A computer has instructions that each require two bus cycles, one to fetch the instruction and one to fetch the data. Each bus cycle takes 10 nsec. And each instruction cycle takes 20 nsec (i.e., the internal processing time is negligible). The computer also has a disk with 2048 512-byte sectors per track. Disk rotation time is 5.0 msec. To what percent of its normal speed is the computer reduced during DMA transfers if each 32-bit DMA transfer takes one bus cycle?

Simple Bus cycle stealing.

How often is a one Byte DMA transfer needed?

5.0 msec/track / (2048*512) bytes/track / 4 bytes/word = 5.0x10^{-3} / 2^{18} = 19.07 nsec/word

Cycle stealing = 19.07 / 39.07 \approx 48% 

A little more than every other bus cycle must be “stolen” from the CPU for the DMA transfer. Therefore, the CPU can only operate at approximately a 50% rate. If you get into details, the processing rate is at 47.6% during DMA cycles.
Designing an I/O system

The general approaches to designing I/O system

- Find the weakest link in the I/O system, which is the component in the I/O path that will constrain the design. Both the workload and configuration limits may dictate where the weakest link is located.

- Configure this component to sustain the required bandwidth.

- Determine the requirements for the rest of the system and configure them to support this bandwidth.
Example Problem

A CPU can sustain 3 billion instructions per second and averages 100,000 instructions in the OS per I/O operation.

The Memory backplane bus is capable of sustaining a transfer rate of 1000 MB/s. SCSI Ultra320 controllers have a transfer rate of 320 MB/s and can accommodate up to 7 disk drives with a read/write bandwidth of 75 MB/s and an average seek plus rotational latency of 6 ms.

If the workload consists of 64 KB sequential reads and the user program requires 200,000 instructions per I/O operation, what’s the maximum I/O rate and the number of disks and SCSI controllers needed (ignoring disk conflicts)?
Example Problem

CPU
- 3 GHz
- 1000 MB/s

Memory
- 320 MB/s

SCSI
- 75 MB/s

Disk
- 3 GB/s
Example Problem

The two fixed component of the system are the memory bus and the CPU. Let’s first find the I/O rate that these two components can sustain and determine which of these is the bottleneck.

Maximum instruction rate = Instruction execution rate / Instruction per IO

\[ = 3 \times 10^9 / [(200 + 100) \times 10^3 ] = 10000 \text{ IO’s/sec.} \]

Maximum IO rate of the bus = Bus BW / Bytes per IO = \(1000 \times 10^6 / 64 \times 10^3\) = 15625 IO’s/sec

The **bus is the bottleneck**, so we can now configure the rest of the system to perform at the level dictated by the bus, 15625 IO’s/sec
Example Problem

Now, we can determine how many disks we need to be able to Accommodate 15625 IO’s/sec. To find the number of disks, we first find the time per I/O operation at the disk:

Time per IO at disk = Seek(rotational) time + transfer time:

\[= 6\text{ms} + \left(\frac{64\text{KB}}{75\text{MB/sec}}\right) = 6.9\text{ms}\]

This means each disk can complete 1000ms/6.9ms, or 146 IO’s/sec.

To saturate the bus, the system need 10000/146 \approx 69 \text{ disks}.\]
Example Problem

To compute the number of SCSI buses, we need to know the average transfer rate per disk, which is given by:

Transfer rate = Transfer size / Transfer time = 64KB / 6.9ms = 9.56MB/sec

Assuming the disk accesses are not clustered so that we can use all the bus bandwidth, we can place 7 disks per bus and controller.

This means we will need 69/7, or **10 SCSI buses and controllers.**
Bus Example: PCI-e

- Developed by Intel
- Peripheral Component Interconnect
- PCI Express architecture is a high performance, IO interconnect for peripherals.
- A **serial point-to-point** interconnect between two devices
- **PCI-Express slots** also accepts older PCI cards
- Data sent in packets
- Synchronous
- No shared bus but a **shared switch**
Bus Example: PCI-e

<table>
<thead>
<tr>
<th>Link Width</th>
<th>x1</th>
<th>x2</th>
<th>x4</th>
<th>x8</th>
<th>x12</th>
<th>x16</th>
<th>x32</th>
</tr>
</thead>
<tbody>
<tr>
<td>Aggregate BW (GBytes/s)</td>
<td>0.5</td>
<td>1</td>
<td>2</td>
<td>4</td>
<td>6</td>
<td>8</td>
<td>16</td>
</tr>
</tbody>
</table>
HyperTransport is often used as the system bus architecture of modern AMD CPU’s and the associated Nvidia nForce motherboard chipsets. HyperTransport has also been used by IBM and Apple for the Power Mac G5 machines, as well as a number of modern MIPS systems.

PCI express (PCI-e) is a high-speed serial computer expansion bus standard designed to replace the older PCI, PCI-X, and AGP bus standards.
Source: National Instruments
PCle Card

- Is any device connected to PCle bus

Graphics card PCle (x16)
Source: National Instrument
Bus Example: USB

- Universal Serial Bus
- Asynchronous \(\rightarrow\) clockless
- Industry standard developed in the 1990s
- Communicates data and power
- USB 3.0
  - Introduced 2008
  - Backward compatible
  - Increase the data transfer rate (up to 5 Gbit/s)
  - Decrease power consumption
  - Increase power output
- USB 3.1 releases July 2013
Bus Example: USB

- **Host**: Initiates all transactions and bandwidth usage. The host controls most of the protocol complexity → allowing for cheaper slave devices to be produced.
- **Slave**: A peripheral USB device
- **Hub**: A device that contains multiple ports.
  - There will always be a root hub. This is the hub that contains the ports connected to the host.
  - We can have a tree of hubs till 5 levels.
Example: USB

- Host
- Root Hub
- HUB
  - Keyboard
  - Speaker
  - Printer
  - HUB
  - Disk
USB

USB evolution:

1.X – early version that did not allow for extension cables or pass-through monitors, due to timing and power limitations

2.0 – added a higher maximum signaling rate of 480 Mbit/s, mini-A and B connectors and battery charging via current up to 1.5 A and allowing a maximum current of 5 A

3.0 – November 2008. The standard defines a new SuperSpeed mode with a signaling speed of 5 Gbit/s and, due to encoding overhead, usable data rate of up to 4 Gbit/s (500 MB/s).

3.1 – January 2013 updates speed of USB 3.0 to 10 Gbit/s. It is backwards compatible with USB 3.0 and 2.0. It allows for higher currents and supply voltages from compliant hosts – up to 2 A at 5 V (for a power consumption of up to 10 W), and optionally up to 5 A at either 12 V (60 W) or 20 V (100 W).
Example: USB

When a USB device is attached to or removed from the USB, the host uses a process known as bus enumeration to identify and manage the device state changes necessary. When a USB device is attached to a powered port, the following actions are taken:

1. The hub to which the USB device is now attached informs the host of the event via a reply on its status change pipe. At this point, the USB device is in the Powered state and the port to which it is attached is disabled.

2. The host determines the exact nature of the change by querying the hub.

3. Now that the host knows the port to which the new device has been attached, the host then waits for at least 100 ms to allow completion of an insertion process and for power at the device to become stable. The host then issues a port enable and reset command to that port.

4. The hub performs the required reset processing for that port. When the reset signal is released, the port has been enabled. The USB device is now in the Default state and can draw no more than 100 mA from VBUS. All of its registers and states have been reset and it answers to the default address.

5. The host assigns a unique address to the USB device, moving the device to the Address state.

6. Before the USB device receives a unique address, its Default Control Pipe is still accessible via the default address. The host reads the device descriptor to determine what actual maximum data payload size this USB device’s default pipe can use.

7. The host reads the configuration information from the device by reading each configuration zero to n-1, where n is the number of configurations. This process may take several milliseconds to complete.

8. Based on the configuration information and how the USB device will be used, the host assigns a configuration value to the device. The device is now in the Configured state and all of the endpoints in this configuration have taken on their described characteristics. The USB device may now draw the amount of VBUS power described in its descriptor for the selected configuration. From the device’s point of view, it is now ready for use.

When the USB device is removed, the hub again sends a notification to the host. Detaching a device disables the port to which it had been attached. Upon
Example: USB

Source: ATMEL
Cooling: Air

- Case fans come in a variety of sizes.
  - Most cases are designed to use 80 mm, 90 mm, and 120 mm fans.
- CPU’s, video cards, power supply, and other components often use their own dedicated fan(s).
- Heatsinks are normally constructed from copper and/or aluminum and directly contact microchips on a circuit board.
- A fan blows air across the heatsink which transfers heat absorbed from the CPU into the air.
Cooling: Air

Case Fans
Cooling: Air

CPU Heatsinks and Fans
What’s Bad About Air Cooling

• Fans can be loud.
• Air cooling is will not cool as well as the other methods such as liquid cooling.
• You have to clean the fans.
• Needs a basic understanding of thermodynamics to be efficient.
Cooling: Water

- Uses water pushed through a radiator to cool computer components via a pump, reservoir, and tubing.
- Used to cool high end servers, desktops, and super computers like the Cray systems.
- Can be made to a single component or to all components such the north and south bridge chipsets.
- Around 34% more efficient than air cooling.
Processor Socket

• Compatible with specific type(s) of microprocessors.
• How chips are attached to a motherboard (more on that later)
## Motherboards Based on Packaging

<table>
<thead>
<tr>
<th>Type</th>
<th>For</th>
</tr>
</thead>
<tbody>
<tr>
<td>LGA 1156</td>
<td>Intel Core i3, i5, and i7</td>
</tr>
<tr>
<td>AM3</td>
<td>AMD Phenom II and AMD Athlon II</td>
</tr>
<tr>
<td>LGA 775</td>
<td>Intel Core 2 Duo, Intel Core 2 Quad and Intel Xeon processor</td>
</tr>
<tr>
<td>939</td>
<td>AMD Athlon 64, Athlon 64 FX, Athlon 64 X2 and Opteron</td>
</tr>
</tbody>
</table>
How Chips Are Mounted on Motherboards

• Packaging technology
• PGA (Pin-Grid-Array):
  – Pins are arranged in a regular array on the underside of the package.
  – Chip mounted on the board using the through hole method or inserted into a socket.
  – Used in most AMD processors
• LGA (Land-Grid-Array):
  – Pins on the socket rather than the chip
  – Newer Intel processors and many AMD Opteron
Intel Pentium MMX

Source: http://www.cpu-world.com/CPUs/Pentium/
Source: http://www.computer-hardware-explained.com/images/CPU-socket.jpg
LGA

LGA 1156

Source: http://www.anandtech.com/show/2832/2
# Motherboards Based on Dimensions

<table>
<thead>
<tr>
<th>Type of Motherboard</th>
<th>Description</th>
</tr>
</thead>
</table>
| AT                  | - Oldest type of motherboard still used in some systems  
                     - Uses P8 and P9 power connections (see Figure 5-1)  
                     - Measures 30.5 cm × 33 cm (12 inches × 13 inches) |
| Baby AT             | - Smaller version of AT. Small size is possible because motherboard logic is stored on a smaller chip set.  
                     - Uses P8 and P9 power connections  
                     - Measures 33 cm × 22 cm (12 inches × 8.7 inches) |
| ATX                 | - Developed by Intel for Pentium systems  
                     - Has a more conveniently accessible layout than AT boards  
                     - Includes a power-on switch that can be software-enabled and extra power connections for extra fans  
                     - Uses a P1 connector (see Figure 5-1)  
                     - Measures 30.5 cm × 24.4 cm (12 inches × 9.6 inches) |
| Mini ATX            | - An ATX board with a more compact design  
                     - Measures 28.4 cm × 20.8 cm (11.2 inches × 8.2 inches) |

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What to Look for in Motherboards?

- Form-factor
- Socket
- Chipset
  - Latest from Intel: Z77, Z79, Z87
  - Latest from AMD: A85X, 990X, and 990FX
- SLI/Crossfire support
  - If you want to connect more than one video card.
- Ports
- Slots
  - Must be careful whether all are enabled
  - Example: PCIe can be x16 in length but x8 electrically.
- Backup BIOS (nice to have!)
- POST LED (displays POST code while booting)
CPU’s What Do You Look For?

• Socket
  – If you plan to upgrade, don’t pick the socket with least amount of life left.
  – Example: for Intel: pick LGA1150 or LGA1156 instead of LGA1155
  – Example: for AMD: AM3+ is nice from budget dual-core up to eight-core chips.

• Core count
  – Better than frequency these days as a measure of potential performance
  – More cores are better if you can use them.
What to Look For?

- **Clock frequency**
  - Good only for comparing processors of the same family
- **Cache**
  - In many cases, chips are the same! That is: an chip 6MB of L2 cache is usually the same as 8MB cache but the 2MB are either defective or turned off!
  - How good a large cache is depends on the workload.
- **Integrated graphics**
  - Much slower than the discrete GPUs
# Processor Numbering System: Intel As Example

![Processor numbering system diagram](image)

<table>
<thead>
<tr>
<th>Alpha Suffix</th>
<th>Correct Trademark Usage</th>
</tr>
</thead>
<tbody>
<tr>
<td>MX</td>
<td>Intel® Core™ i7-4900MX processor</td>
</tr>
<tr>
<td>MQ</td>
<td>Intel® Core™ i7-4900MQ processor, Intel® Core™ i7-4702MQ processor</td>
</tr>
<tr>
<td>M</td>
<td>Intel® Core™ i7-4600M processor, Intel® Core™ i5-4300M processor</td>
</tr>
</tbody>
</table>

Processor Numbering System: AMD Opteron as Example

• AMD Opteron processors are described by a three-digit model number.
• The first number indicates the maximum scalability of the processor.
  – AMD Opteron 100 vs AMD Opteron 800
• The second two digits indicate relative performance within the series.
  – Dual-Core AMD Opteron processor Model 880 outperforms a Dual-Core AMD Opteron processor Model 875.
GPU - CPU comparison

- AMD (GPU)
- NVIDIA (GPU)
- Intel (CPU)

Many-core GPU
Multi-core CPU

Courtesy: John Owens
GPUs Today

• Are general purpose and not only for graphics
• Discrete
  – separate chip on-board like all Nvidia GPUs and AMD Radeo
• Integrated
  – With the CPU on the same chip like the GPU in Intel Sandy Bridge and Ivy Bridge
What to Look for?

• The amount of GPU memory
  – Also called frame-buffer
  – The larger the memory the higher the resolution the GPU can handle.
  – Ranges from 1GB in low-end to 6GB in high-end
  – Example: you will need 3GB-4GB memory for 2560x1600 with decent frame rates
  – Anti-Aliasing (AA): smoothing out edges \( \rightarrow \) may require more memory for lower rendered resolution.

• How many cores?
  – Cores here are simpler than cores in a multicore chips
  – Called stream processors by AMD and CUDA cores by Nvidia

• The two big players: Nvidia and AMD
  – built on different architectures so we cannot compare them
  – This means more cores on an AMD GPU than Nvidiia GPU does not necessarily mean the former is faster.
GPU cards

Nvidia cards

ATI cards
What to Look for?

• Memory bus
  – Path between GPU itself and the video card memory
  – Bus width and speed of memory \(\rightarrow\) bandwidth (GB/s) \(\rightarrow\) more is better
  – Example:
    • GTX 680: 6GHz memory and 256-bit interface \(\rightarrow\) 192.2 GB/s
    • GTX Titan: 6GHz memory and 384-bit interface \(\rightarrow\) 288.4 GB/s
  – Since most modern gaming GPUs use 6GHz memory, the bus width is the one that makes the difference.
What to Look for?

• Power requirements
  – Most GPUs use PCIe power connectors (6-pin or 8-pin)
  – Most high-end cards will draw 100-200W of power under load → you may need 500-650W PSU (power supply unit) for your entire computer system.

• Display connectors
  – Connects GPU to the display
  – Example:
    • DVI: single-link and dual-link
    • HDMI: versions 1.1, 1.2, 1.3, and 1.4 → for higher resolutions

• The architecture: Fermi and Kepler (latest)
Example: Nvidia Kepler Architecture

Example: Nvidia Chip GK110 Based on Kepler Architecture

• 7.1 billion transistors
• More then 1 TFlop of double precision throughput
  – 3x performance per watt of Fermi
• New capabilities:
  – Dynamic parallelism
  – Hyper-Q
  – Nvidia GPUDirect
System memory - What to look for?

• Capacity
• Clock speed
  – in MHz (e.g. DDR3/1866 runs at 1.866MHz)
  – DDR → double data rate : DDR2, 3, and 4
• Registered DIMMs (aka Buffered DIMMs)
  – Extra chip on the module to take some load off
    the memory controller
• ECC RAM: Error-Correcting Control
  – Make sure the CPU supports it if you want to
    use ECC RAM.
**Memory**

**Micron 1-Gbit DRAM**

**DRAM evolution** over the years:

- Asynchronous DRAM
- Video DRAM (VRAM)
- Fast page mode DRAM (FPM)
- Extended data out DRAM (EDO)
- Burst EDO (BEDO)
- Synchronous DRAM (SDRAM)
  - Single data rate (SDR)
  - Double data rate (DDR)
- Direct RAMBUS DRAM (DRDRAM)
- Pseudostatic DRAM (PSDRAM)
- Reduced latency DRAM (RLDRAM)
- 1T DRAM

**DRAM Implementations**

- Single inline memory module (SIMM)
- Dual inline memory module (DIMM)
- Error correcting (ECC)
- Buffered
- Fully buffered (FB-DIMM)
- Registered
- Unregistered
Storage

• SSD (Solid-Sate Disks)
  – Usually using NAND flash
    • SLC, MLC, or TLC (Single, Multi, Triple-level cell) \(\rightarrow\) how many values it can hold in a cell at one time \(\rightarrow\) cost vs capacity
  – Performance depends on the controller that:
    • Reads and writes data from flash
    • optimizes the drive
    • performs routing garbage collection
    • Comes from: LSI Sandforce, Smasung, OCZ, …
  – Over-provisioning = size taken from total capacity for drive maintenance
    • Example: If your drive is listed as 240GB then it has 16GB reserved for over-provisioning
Storage

Jumpers on back of IDE hard disk drive IDE cable

Back of IDE hard disk drive

IDE interface cable  Jumpers  Power connection

http://www.computerhope.com

40-Pin IDE IDC Connector and cable

http://www.computerhope.com

Serial ATA cables

SATA Type A  eSATA

Serial ATA expansion ports
Storage

- HDD (Hard-Disk Drives)
  - capacity
  - RPM (Rotation-per-Minute)
  - Cache size
    - Small memory with the disk (standard: 64MB)
    - Used as buffer
  - Platters
    - HDD stores data on several platters where data is stored on both-sides
    - Highest density platter = 1TB
    - The higher the density the better the performance of the disk
- NCQ Technology
  - Native command queuing
  - help the drive priorities data requests for efficient processing
Other peripherals - LAN interface

The most common type of network is a wired network using Ethernet cables and hardware. For this type of network, you need to install and configure a network interface card (NIC) in each of your PCs.

Bluetooth (IEEE 802.15.1) is a wireless technology standard for exchanging data over short distances. It uses the ISM band from 2.4 to 2.485 GHz. It was invented by telecom vendor Ericsson in 1994 and was originally conceived as a wireless alternative to RS-232 data cables.

Wifi (IEEE 802.11) is a set of media access control (MAC) and physical layer (PHY) specifications for implementing wireless local area network (WLAN) computer communication in the 2.4, 3.6, 5 and 60 GHz frequency bands.
Audio sound card

All motherboards on the market come with embedded sound cards, or onboard audio. The problem is that since motherboards need to be small enough to fit into your tower, they have limited space for the sound card. As such, onboard audio is not able to produce the same quality of audio as a dedicated sound card.

Dedicated sound cards have a number of improved or added features, which in turn produce better sound quality all around. Features like higher signal-to-noise ratios, lower harmonic distortion, 24-bit sample rates, 192-kHz resolution and surround sound.
CODEC Chip Types

There are many different types of codec chips. Examples include a (Wolfson)WM8731 audio codec chip, (Analog Devices)ADV202 video codec chip, MP3 codec chip, and a WMV codec chip. A WM8731 audio codec chip is designed for use in portable digital audio sets. A WM8731 audio chip works on a software algorithm that requires less power and uses high quality audio codec integration.

A user can download audio codec logic and implement it in the circuit. An ADV202 video codec chip is used in applications that require high-quality and image compressed video. An MP3 codec chip is also commonly known as QuickTime video codecs.

An MP3 codec chip or QuickTime video codecs are designed specifically for use in a high-level of integration and performance in speech and audio applications. A WMV codec chip is abbreviated for Windows Media and is an audio codec chip. A WMV codec chip can be used interchangeably either as an audio or video chip. Other codec chips are also commonly available.
There are several ways in which codec chips function. Codec IC chips work by receiving signals in the form of assembly language and then interpreting it into high-level language. The operations are then performed on the basis of received input signals.

A WM8731 audio codec chip requires resistance power ranging from 50mW on 16Ohms and supply voltage of range from 1.42 to 3.6 volts. A WM8731 audio codec chip also requires a sampling frequency ranging from 8 to 96 KHz. An ADV202 video codec chip operates in the temperature range of -40 to 85 ºC and requires a 2.5 to 3.3 volt of power supply.

An MP3 codec chip uses 4K * 20bit program code. The flash memory of an MP3 codec chip requires 2.7 to 3.3 volts supply for its operation. A WMV codec chip requires an operating voltage of 2.5 volts and power of 40mW. Codec chips are designed and manufactured to meet most industry specifications.
Bluetooth Smart technology operates in the same spectrum range (the 2.400 GHz-2.4835 GHz ISM band) as Classic Bluetooth technology, but uses a different set of channels. Instead of the Classic Bluetooth 79 1-MHz channels, Bluetooth Smart has 40 2-MHz channels. Within a channel, data is transmitted using Gaussian frequency shift modulation, similar to Classic Bluetooth's Basic Rate scheme. The bit rate is 1Mbit/s, and the maximum transmit power is 10 mW. Further details are given in Volume 6 Part A (Physical Layer Specification) of the Bluetooth Core Specification V4.0.

Bluetooth Smart uses frequency hopping to counteract narrowband interference problems. Classic Bluetooth also uses frequency hopping but the details are different; as a result, while both FCC and ETSI classify Bluetooth technology as an FHSS scheme, Bluetooth Smart is classified as a system using digital modulation techniques or a direct-sequence spread spectrum.
# Bluetooth & Bluetooth LE

<table>
<thead>
<tr>
<th>Technical Specification</th>
<th>Classic Bluetooth technology</th>
<th>Bluetooth Smart technology</th>
</tr>
</thead>
<tbody>
<tr>
<td>Distance/Range (theoretical max.)</td>
<td>100 m (330 ft)</td>
<td>&gt;100 m (&gt;330 ft)</td>
</tr>
<tr>
<td>Over the air data rate</td>
<td>1–3 Mbit/s</td>
<td>1 Mbit/s</td>
</tr>
<tr>
<td>Application throughput</td>
<td>0.7–2.1 Mbit/s</td>
<td>0.27 Mbit/s</td>
</tr>
<tr>
<td>Active slaves</td>
<td></td>
<td>7</td>
</tr>
<tr>
<td>Security</td>
<td>56/128-bit and application layer user defined</td>
<td>128-bit AES with Counter Mode CBC-MAC and application layer user defined</td>
</tr>
<tr>
<td>Robustness</td>
<td>Adaptive fast frequency hopping, FEC, fast ACK</td>
<td>Adaptive frequency hopping, Lazy Acknowledgement, 24-bit CRC, 32-bit Message Integrity Check</td>
</tr>
<tr>
<td>Latency (from a non-connected state)</td>
<td>Typically 100 ms</td>
<td>6 ms</td>
</tr>
<tr>
<td>Minimum total time to send data (det.battery life)</td>
<td>100 ms</td>
<td>3 ms [32]</td>
</tr>
<tr>
<td>Voice capable</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Network topology</td>
<td>Scatternet</td>
<td>Scatternet</td>
</tr>
<tr>
<td>Power consumption</td>
<td>1 W as the reference</td>
<td>0.01 to 0.5 W (depending on use case)</td>
</tr>
<tr>
<td>Peak current consumption</td>
<td>&lt;30 mA</td>
<td>&lt;15 mA</td>
</tr>
<tr>
<td>Service discovery</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Profile concept</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Primary use cases</td>
<td>Mobile phones, gaming, headsets, stereo audio streaming, smart homes, wearables, automotive, PCs, security, proximity, healthcare, sports &amp; fitness, etc.</td>
<td>Mobile phones, gaming, PCs, watches, sports and fitness, healthcare, security &amp; proximity, automotive, home electronics, automation, Industrial, etc.</td>
</tr>
</tbody>
</table>