The PCI bus
Main features

- coupling of the processor and expansion bus by means of a bridge,
- 32-bit standard bus width with a maximum transfer rate of 133 Mbytes/s,
- expansion to 64 bits with a maximum transfer rate of 266 Mbytes/s,
  - PCI-64/66 532 Mbytes/s, PCI-X 64/133 1064 Mbytes/s
- supporting of multi-processor systems,
- burst transfers with arbitrary length,
- supporting of 5 V and 3.3 V power supplies,
- write posting and read prefetching,
- multimaster capabilities,
- operating frequencies from 0 MHz to a maximum of 33 MHz,
  - PCI-66 3.3V only, PCI-X 100MHz-133MHz
- multiplexing of address and data bus reducing the number of pins,
- supporting of ISA/EISA/MCA,
- configuration through software and registers,
- processor independent specification
Block diagram of a PCI bus system

Processor/Main Memory System

Coprocessor → CPU → Cache → Main Memory

PCI Bridge

PCI Bus

SCSI host adapter → Interface to Expansion Bus → LAN adapter → I/O → Graphics adapter

Expansin Bus (ISA/EISA)

Bus Slot → Bus Slot → Bus Slot → Bus Slot
PCI Chipset on Motherboard
PCI bus
PCI bus Signals

- **ACK64**: acknowledge 64-bit transfer
- **AD31-AD0**: 32 address and data pins form the multiplexed PCI address and data bus
- **C/BE3#-C/BE0#:** command and byte-enable
- **CLK**: PCI clock signal
- **DEVSEL#:** device select
- **FRAME**: 
- **GNT#:** grant
- **IDSEL**: device select during configuration
- **INTA#, INTB#, INTC#, INTD#:** interrupt signals
- **IRDY#:** initiator ready
- **LOCK**: defines an atomic access
- **PAR**: even parity for AD31-AD0 and C/BE3#-C/BE0#
- **PERR#:** parity error
- **PRSNT1#, PRSNT2#:** indicate that an adapter is installed
- **REQ#:** request signal to the bus arbitration unit
- **REQ64#:** 64-bit transfer request
- **RST**: resets all PCI units
- **SBO#:** snoop backoff, indicates a hit to a modified cache line
- **SDONE**: snoop done
- **SERR#:** system error
- **STOP**: target-abort
- **TCK, TDI, TDO, TMS, TRST#:** JTAG boundary scan test signals
- **TRDY**: target ready
- **64 bit expansion**
  - **AD63-AD32**: 32 address and data pins form the expansion of the multiplexed PCI address and data bus
  - **C/BE7#-C/BE4#**
  - **PAR64**: even parity for the 64bit expansion
The PCI read transfer burst
The PCI write transfer burst.
PCI bus features

- Bus Arbitration
  - Parallel arbitration
  - Hidden arbitration
  - Arbitration algorithm is not defined
- DMA
  - Burst transfers
- Interrupts
  - INTA# activated
  - Data: interrupt vector
PCI Bus Cycles

- INTA sequence (0000)
- special cycle (0001)
- I/O read access (0010)
- I/O write access (0011)
- memory read access (0110)
- memory write access (0111)
- configuration read access (1010)
- configuration write access (1011)
- memory multiple read access (1100)
- dual addressing cycle (1101)
- line memory read access (1110)
- memory write access with invalidation (1111)
### PCI Configuration Address Space

The PCI Configuration Address Space is a 64-byte header followed by 192 bytes available for PCI unit configuration.

#### 64 Byte Header
- **Unit ID**
- **Manufacturer ID**
  - allocated by PCI SIG
- **Status**
- **Command**
- **Class code**
- **Revision**
- **BIST**
- **Header**
- **Latency**
- **CLS**

#### 192 Bytes Available for PCI Unit
- **Base Address register**
- **Reserved**
- **Reserved**
- **Reserved**
- **Expansion ROM Base Address**
- **Reserved**
- **Reserved**
- **Max. Lat.**
- **Min. GNT**
- **INT-Pin**
- **INT-Line**

#### Key Attributes
- **Manufacturer ID** identifies the manufacturer.
- **Unit ID, revision** identifies the specific unit.
- **Class code** identifies the type of PCI unit.

![Diagram of PCI Configuration Address Space](image-url)
Status and Command Registers

• Status:
  – PER: Parity error
  – SER: System error
  – MAB: Master abort
  – TAB: Target abort received
  – STA: Target abort signaled
  – DEVTIM: DEVSEL timing
    • 00=fast 01=medium
    10=slow 11=reserved
  – DP: Data parity error
  – FBB: Fast back-to-back cycles supported/unsupported

• Command:
  – BEE: Fast back-to-back cycles
    (Back-to-Back Enable)
  – SEE: SERR Enable
  – WC: Wait cycle control
  – PER: Parity error (Parity Error Response)
  – VPS: VGA palette snoop
  – MWI: Memory write access with invalidation
  – SC: Special cycle
  – BM: Busmaster
  – MAR: Activate/deactivate Memory address area
  – IOR: Activate/deactivate I/O address area
PCI Configuration Address Spaces

- Configuration Mechanism #1
  - CONFIG-ADDRESS (0cf8h) and CONFIG-DATA (0cfch) registers are defined in the I/O area

- Configuration Mechanism #2 (for PC systems)
  - 4k I/O address range between c000h and cffffh
PCI Base Address Registers

For Memory Address Space

<table>
<thead>
<tr>
<th>31</th>
<th>16</th>
<th>15</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Base Address</td>
<td>PRF</td>
<td>Type</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

For I/O Address Space

<table>
<thead>
<tr>
<th>31</th>
<th>16</th>
<th>15</th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Base Address</td>
<td>PRF</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

For Expansion ROM Address Space

| 31 | 16 | 15 | 11 | 10 | | | |
|----|----|----|----|----|---|---|
| Base Address | Reserved | | | | | AD |

- PRF: Prefetching not possible/prefetching possible
- Type: Positioning type
  - 00=any 32-bit address, 01=less than 1M, 10=any 64-bit address, 11=reserved
- AD: Address decoding and expansion ROM deactivated/activated
Evolution of PC buses
The PCI Express Bus

• Point to point protocol
  – x1, x2, x4, x8, x12, x16 or x32 point-to-point Link

• Differential Signaling
Electrical Physical Layer Showing Differential Transmitter and Receiver

Transmitter is AC coupled to receiver
DC common mode impedance is 50 Ohms
Differential impedance is 100 Ohms
Coupling capacitor is between 75-200 nF
PCI Express System
PCI Express Properties

• Packet Based Protocol

• Bandwidth and Clocking
  – 2.5 Gbits/sec/lane/direction
  – 8b/10b encoding
  – 250 Mbytes/sec/lane/direction

• Address Spaces
  – Memory
  – I/O
  – Configuration (extended from 256 Bytes to 4 Kbytes)
PCI Express Transactions

- Transactions
  - memory read / write
  - I/O read / write
  - configuration read / write
  - new transaction type: Message transactions

- Transaction Model
  - posted (split transaction communication)
  - non-posted
PCI Express Properties

- Quality of Service (QoS)
  - deterministic latencies and bandwidth
- Traffic Classes (TCs)
  - TCs can move through the fabric with different priority
- Virtual Channels (VCs)
  - Each Traffic Class is individually mapped to a Virtual Channel
- Interrupt Handling
  - Virtual wires
- Power Management
  - device power states: D0, D1, D2, D3-Hot and D3-Cold
    - D0 is the full-on power state
    - D3-Cold is the lowest power state.
  - Link power states: L0, L0s, L1, L2 and L3
- Hot Plug Support
- PCI Compatible Software Model
PCI Express Topology
PCI Express Device Layers
PCI Express Transaction Layer Packets

PCI Express Packet Format

- Framing
- Sequence Number
- Header
- DATA
- ECRC
- LCRC
- Framing

- 4-4096 bytes

- TRANSACTION LAYER (12 or 16 bytes overhead)
- DATA LINK LAYER (8 bytes overhead)
- PHYSICAL LAYER (20 percent 8b/10b encoding overhead)
The PCI Express AS protocol is inserted into a base PCI Express format. The data payload, in this case a PCI Express base packet, could be data in any protocol format as PCI Express AS is protocol agnostic. The PCI Express AS protocol requires a start indicator, or comma, and an AS header that contains the PI or Protocol Interface and the routing path of the AS packet.