The Design of a Digital Satellite Set-Top Box
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## Component List & Cost

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At the early stages of this project, I asked myself what are Digital Set-top boxes, STB herein? Never mind ever thinking of the design of one. Reading Gerald O’Driscoll’s “The Essential Guide to Digital Set-top Boxes and Interactive TV” provided me with a robust fundamental understanding of STBs in terms of their functionality. In his book, a STB is defined as “a consumer electronics device used to decode and tune digital signals and convert them to a format that is understood by your television.” Their primary features may be classified as follows: (1) decodes the incoming digital signal; (2) verifies access rights and security levels; (3) displays cinema-quality pictures on your TV set; (4) outputs digital surround sound; and (5) processes and renders Internet and interactive TV services. In a Satellite set-top box, the tuner receives the satellite’s transmission and extracts a particular channel. A demodulator then receives the signal and converts it into binary format. It may also perform an error check at this stage as well. Once cleared, the binary signal is sent to a demultiplexer where audio, video, and data are isolated from the signal, and subsequently sent to the appropriate decoder. The demultiplexer may also determine access rights to the various services. The decoders’ functions are to transform their respective incoming binary stream into the proper viewable television format.

The building blocks of a digital broadcasting system essentially consists of receiving digital signals, compression and encoding, modulation, conditional access system, network transmission technologies and network management. On the receiving end the main components of the STB are:

- system bus,
- tuner(s),
modulators and demodulators,
demultiplexer and decryptor,
decoders,
graphics processor,
CPU and memory
storage devices,
physical interfaces, and
physical characteristics. [1]

All of the primary components of the design will be connected on a system board. The bus that will be used is the Intel based PCI. The system bus will have the same width as the processor -- 32 bits. The bus speed will be able to support 133 MHz, since the design does not include Intel’s NetBurst micro-architecture, which could have meant greater speeds.

An IBM copper-based 750FX Power PC processor will lay at the heart of the design. In terms of functionality and processing, the CPU is the most important element of a digital set-top box. The general functions that the processor will provide are:

- initializes the various set-top hardware components;
- processes a range of Internet and interactive TV applications;
- monitors and manages hardware interrupts;
- fetches data and instructions from memory; and
- runs various programs.

The tuner in this design will be able to access QAM-, OFDM-, and QPSK-based networks. In addition to receiving inputs from digital networks, the tuner will be able to
of tuning analog broadcasts as well. Tuners may be summed up by the three categories below:

- **Broadcast In-band (IB) Tuner.** Once the signal arrives from the physical transmission media, the IB tuner will isolate a physical channel from a multiplex of channels and convert to baseband. The term baseband is used to describe a single channel or digital signal, extracted from a broadband signal which is basically a stream of multiple channels.

- **Out of Band (OOB) Tuner.** This type of tuner facilitates the transfer of data between the head-end systems and the set-top box. They are widely used in cable set top boxes for providing subscribers with a medley of interactive services.

- **Return Path Tuner.** This tuner allows a subscriber to activate the return path and send data back to the interactive services provider.

The demodulator will receive the baseband output signal from the tuner and sample and convert it to a digital binary signal. This binary signal has audio, video, and data components. After the streams are checked for errors they are forwarded to the demultiplexer. A modulator reverses the action of a demodulator, but is used to send signals out from the set-top box.

MPEG-2 data packets will consist of a Packet ID (PID) that would identify a packet as containing audio, video, or interactive service formats. Each format is sent to a specific decoder that would have the capability to decode that specific format. A video decoder will translate the video packets into a sequence of pictures to be displayed on the television set. The compressed audio bit-stream will be decoded by the audio decoder. Once the MPEG-2 stream is translated it will be presented to a set of speakers. Finally, a data decoder will decode the data.

The second processor used in the design will be dedicated to graphics. The graphics processor will render a range of Internet file formats and interactive TV file
formats. Once it is rendered, the graphics file will overlay the standard video display on TV.

Memory, obviously, is needed in the design. Most of the elements within the STB will need memory to be able to perform their tasks. The graphics engine, video decoder, and the descrambler will all require a certain amount of memory to fulfill their specific functions. SRAM will be used to support time critical tasks such as MPEG processing and DRAM for interactive applications.

Hard disks will also be included in the design for user memory space, since the ability to locally store and retrieve information is one of the most important concerns for a customer with digital TV service. The disk interface technology that will be incorporated into this design is Small Computer Systems Interface (SCSI); also know as “skuzzy”. Though they are more expensive, in general, skuzzy hard drives would offer subscribers with faster access and data retrieval times than the competition brand of hard drives – Integrated Drive Electronics (IDE).

As far as physical interfaces for the STB, there is a wide range of available choices. They are classified in the following categories:

- modems,
- high-speed multimedia interfaces,
- RS232,
- common interface,
- TV and VCR interfaces,
- smart card readers,
- remote controls,
- IR blasters, and
- wireless keyboards.

A modem will be incorporated into the design to facilitate the implementation of two-way interactive services. Once connected and activated, the modem is able to utilize the return path for various uses, such as:
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- sending requests to Web servers on the Internet,
- enabling set-top users to upload files and send e-mail; and
- facilitating two-way interactive TV services, such as video on demand.

This STB will incorporate a high speed multimedia interface. It will be able to communicate in real time with devices, such as camcorders, DVDs, CD players, and musical keyboards. An IEEE 1284 Parallel Port will be included for high-speed bidirectional interface to a printer. Apple Computers’ IEEE 1394 or FireWire Bus Interface Standard will also be included in the design. This networking standard will connect high bandwidth consumer electronic devices such as an STB. It will offer plug-and-play technology which would allow consumer connected devices to be automatically configured.

An RS-232 interface port will be equipped in the design of the STP for serial communications. It will use a D connector with 9 pins and allows connectivity to serial printers, computers, and standard telephone modems.

PCMCIA (Personal Computer Memory Card International Association) card will be used, and is best described as a credit card sized peripheral which has various uses:

- extending the set-top memory capabilities;
- storing and decrypting CAs for multiple service providers;
- adding hard disk space to the set-top box; and
- adding new tuners to the set top box.

These cards are sometimes referred to as point of deployment (POD) modules. It will be made into a separate unit from the STB itself. This will theoretically make the STP interchangeable, which means that it could be sole in the retail channel. [6]
TVs and VCRs will be able to communicate with the STB through two outputs Scart connectors, which will use female-type connectors with 21 pins.

A Smart Card Reader will be deployed for authorization to various digital television services and for e-commerce applications. Remote controls and wireless keyboards will be included in the STB package for the subscriber’s convenience and comfort. A generic layout of an entire Set-top Box system is furnished above as an overview (Source: Texas Instruments).
The table below furnishes all of the components used for the design discussed in the instant report. It also includes the manufacturer, model number, cost, and a technical resource for the product. Each color represents a specific portion of the STB.

<table>
<thead>
<tr>
<th>Component</th>
<th>Manufacturer</th>
<th>Model No.</th>
<th>Cost</th>
<th>Technical Resource</th>
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Table 1: Components & cost used in the design of Digital Set-Top Box
The entire block diagram is furnished here for an overall view of the set-top box design discussed in this paper. This will proceed with a meticulous description of each component within the system.

**Microprocessor: IBM PowerPC 750 FX**

The PowerPC 750FX RISC Microprocessor is capable of delivering the resources for a high performance application such as a set-top-box, while keeping power consumption at a minimum. IBM has also included on-board Error Correction Circuitry (ECC). This processor’s resume is very impressive:

- Branch Processing Unit
  - Four instructions fetched per clock
  - One branch processed per cycle
- Up to one speculative stream in execution, one additional speculative stream in fetch
- 512-entry branch history table (BHT) for dynamic prediction
- 64-entry, 4-way set associative branch target instruction cache (BTIC) for eliminating branch delay slots

■ Decode
  - Register file access
  - Forward control
  - Partial instruction decode

■ Load/store unit
  - One cycle load or store cache access
  - Effective address generation
  - Hits under miss (one outstanding miss)
  - Single-cycle misaligned access within double-word boundary
  - Hits under miss (one outstanding miss)
  - Single-cycle misaligned access within double-word boundary
  - Alignment, zero padding, sign extend for integer register file
  - Floating-point internal format conversion (alignment, normalization)
  - Sequencing for load/store multiples and string operations
  - Store gathering
  - Cache and TLB instructions
  - Big and little-endian byte addressing supported
  - Misaligned little-endian support in hardware

■ Dispatch unit
  - Full hardware detection of dependencies (resolved in the execution units)
  - Full hardware detection of – Dispatch two instructions to six independent units (system, branch, load/store, fixed-point unit 1, fixed-point unit 2 or floating-point)
  - 4-stage pipeline: fetch, dispatch, execute, and complete
  - Serialization control (predispatch, postdispatch, execution, serialization)

■ Fixed-point units
  - Fixed-point unit 1 (FXU1): multiply, divide, shift, rotate, arithmetic, logical
  - Fixed-point unit 2 (FXU2): shift, rotate, arithmetic, logical
  - Single-cycle arithmetic, shift, rotate, logical
  - Multiply and divide support (multi-cycle)
  - Early out multiply
  - Thirty-two 32-bit general purpose registers
Floating-point unit
- Support for IEEE-754 standard single and double-precision floating-point arithmetic
- Optimized for single-precision multiply/add
- Thirty-two, 64-bit floating point registers
- Enhanced reciprocal estimates
- 3-cycle latency, 1-cycle throughput, single-precision multiply-add
- 3-cycle latency, 1-cycle throughput, double-precision add
- 4-cycle latency, 2-cycle throughput, double-precision multiply-add
- Hardware support for divide
- Hardware support for denormalized numbers
- Time deterministic non-IEEE mode

System unit
- Executes CR logical instructions and miscellaneous system instructions
- Special register transfer instructions

L1 Cache structure
- 32K, 32-byte line, 8-way set associative instruction cache
- 32K, 32-byte line, 8-way set associative data cache
- Single-cycle cache access
- Pseudo-LRU replacement
- Copy-back or write-through data cache (on a page per page basis)
- Parity on L1 tags and arrays
- 3-state (MEI) memory coherency
- Hardware support for data coherency
- Non-blocking instruction cache (one outstanding miss)
- Non-blocking data cache (two outstanding misses)
- No snooping of instruction cache

Memory management unit
- 64 entry, 2-way set associative instruction TLB (total 128)
- 64 entry, 2-way set associative data TLB (total 128)
- Hardware reload for TLBs
- 8 instruction BATs and 8 data BATs
• Virtual memory support for up to 4 terabytes (252) virtual memory
• Real memory support for up to 4 gigabytes (232) of physical memory
• Support for big/little-endian addressing

Dual PLLs
• Allows seamless frequency switching

Level 2 (L2) cache
• Internal L2 cache controller and 4K-entry tags: 512KB data SRAMs
• Two-way set-associative, supports locking by way
• Copy-back or write-through data cache on a page basis, or for all L2
• 64-byte sectored line size
• L2 frequency at core speed
• ECC protection on SRAM array
• Parity on L2 tags
• Supports up to 2 outstanding misses (1 data and 1 instruction)
• Supports up to 2 outstanding misses (2 data)

Power
• Low power consumption with low voltage application at lower frequency
• Dynamic power management
• 3 static power save modes (doze, nap, and sleep)
• Thermal Assist Unit (TAU)

Bus interface
• 32-bit address bus
• 64-bit data bus (also supports 32-bit mode)
• Enhanced 60x bus: pipelines consecutive reads to a depth of 2
• Core-to-bus frequency multipliers of 3.5x, 4x, 4.5x, 5x, 5.5x, 6x, 6.5x, 7x, 7.5x, 8x, 8.5x, 9x, 9.5x, 10x, 11x, 12x, 13x, 14x, 15x, 16x, 17x, 18x, 19x, and 20x supported
• Supports 1.8V, 2.5V, or 3.3V I/O modes

Reliability and serviceability
• Parity checking on 60x busses
• ECC checking on L2 cache
- Parity on the L1 arrays
- Parity on the L1 and L2 tags

- Testability
  - LSSD scan design
  - Powerful diagnostic and test interface through Common On-Chip Processor (COP) and IEEE 1149.1 (JTAG) interface

The 750 FX’s block diagram is illustrated here for a simplified overall visual of this processor.

![Block Diagram of the PowerPC 750 FX](image)

**Figure:** Block Diagram of the PowerPC 750 FX

**Graphics Processor: NVIDIA GeForce4 MX**

The NVIDIA GeForce4 MX is an outstanding graphics processor with 32MB of DDR memory. It delivers 1.1 billion textured pixels per second. Its performance was pioneered on high-end scientific and
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engineering workstations. Gaming, which has become the greatest interest in today’s households, is of the utmost quality with hardware transform and lighting (T&L), per-pixel shading and drop-dead gorgeous effects at high resolutions, the NVIDIA GeForce4 MX takes over the transform and lighting calculation functions from the CPU, enabling more robust collision detection, better path algorithms and more realistic physics. [11]

MPEG-2 Decoder: Altera CS6651

The MPEG2 (Motion Pictures Expert Group) methodology provides compression of TV quality digital video. Because it provides such good compression, it has become the standard for digital TV via satellite. [3] The MPEG-2 used in the instant design has the following features:

- Supports progressive scan and interlaced streams
- ISO/IEC 13818-2 (H.262)-compliant
- Main profile at main level (MP@ML)-compliant
- Decodes ISO/IEC11172-2 (MPEG1)
  - Constrained parameter bit streams
- High-performance solution for MPEG2 decoding
  - Supports input bit rates up to 30 Mbits/sec
  - Real time decode and display of MP@ML using a single 27-MHz clock
- Supports PAL and NTSC standard definition television (SDTV) resolutions and frame rates
- Bit stream error detection and recovery
- Glueless interface to external SDRAM
- Capable of standalone stream decoding or host central processing unit (CPU) - controlled operation.
- Fully synchronous design with host shutdown and restart control

This Altera MPEG-2 decoder is definitely a good fit for this high performance application. The block diagram is furnished below:
The CS6651 MPEG-2 decoder is capable of decoding video streams at the MP@ML standard. Pictures are decoded from the video stream and output in the correct display order when the decoder is in default mode. Audio/video synchronization, pan-and-scan and letterbox conversion and various other modes is done by a host CPU. A highly configurable pixel stream direct memory access (DMA) engine provides the output from the core. This engine allows adjustable output video component sequencing and provides external logic with control over the display of the picture. To meet the bandwidth requirements of MP@ML decoding, a dedicated SDRAM chip is used. This is a commodity 64-Mbit SDRAM in 2Mx32 configuration.

**MPEG2 DeMux: Phillips Semiconductors**

An MPEG2 DeMux accepts the digital stream output from the A/D converter, and extracts the system clock reference from the pack header. Using a function that measures progress, the system reference clock is reported. All of the above information is stored in a table that is updated as new stream IDs are found. A progress report is sent to notify the application, which in turn either pre-determines what elementary streams needs to be
sent to the audio and video decoders, or selects the stream on the fly using the progress report’s information.

**Power Distribution Switch: National Semiconductor LM3525**

National’s LM3525 provides Universal Serial Bus standard power switch and over-current protection for all host port applications. A 1 ms delay on fault flag output prevents erroneous overcurrent. This is due to the inrush currents during the hot-plug events. Its features are:

- 1 ms Fault Flag Delay During Hot-Plug Events
- Smooth Turn-On Eliminates Inrush Induced Voltage Drop
- UL Recognized Component: REF # 205202
- 1A Nominal Short Circuit Output Current Protects Notebook PC Power Supplies
- Thermal Shutdown Protects Device in Direct Short Condition
- 500mA Minimum Continuous Load Current
- Small SO-8 Package Minimizes Board Space
- 2.7V to 5.5V Input Voltage Range
- Switch Resistance $\leq 120 \, \text{m}\Omega$ Max. at $V_{IN} = 5\, \text{V}$
- 1µA Max Standby Current
- 100 µA Max Operating Current
- Undervoltage Lockout (UVLO)

**IEEE 1394 Link Layer Controller: Texas Instruments TSB12LV26**

This device is compliant with the PCI Local Bus Specification, PCI Bus Power Management Interface Specification, IEEE Std 1394-1995, and 1394 Open Host Controller Interface Specification. This chip provides the IEEE 1394 link function and is compatible with high serial bus data rates.

**IEEE 1394 Physical Layer Controller: Texas Instruments TSB12LV26**

This will provide the digital and analog transceiver functions needed to implement a one-port node in a cable-based IEEE 1394 network. The cable port incorporates one differential line transceiver. As discussed in class, this will eliminate
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noise transmission. The transceiver includes circuitry to monitor the line conditions as needed for determining connection status, for initialization and arbitration, and for packet reception and transmission. The TSB41AB1 is designed to interface with the TSB12LV26 link layer controller.

**Tuner Infineon TAIFUN TUA6034**

This tuner is the industry's first single chip triple-band tuner integrated circuit (IC) for all global broadcast standards. Infineon’s integrated device will reduce the number of ICs that would be used and simplifies the design of the RF (radio frequency) front-end. [9]

**Audio DACs: Phillips Semiconductor UDA1350AH [10]**

The primary features of the Phillips Audio DAC are:

- 2.7 to 3.6 V power supply
- Integrated digital filter and Digital-to-Analog Converter (DAC)
- Master-mode data output interface for off-chip sound processing
- 256fs system clock output
- 20-bit data-path in interpolator
- High performance
- No analog post filtering required for DAC
- Pre-emphasis information of IEC 958 input bit stream available in L3 interface register and on pins

**Phase-Locked Loop: Motorola MC44BC374T**

In Motorola’s PLL version, block diagram provided below, the channel is set by an I2C compatible bus receiver. The PLL tunes the modulator over the full UHF range. The three main sections illustrated in the block diagram below are:

1. A high speed I2C compatible bus section.
2. A PLL section to synthesize the UHF/VHF output channel frequency from an integrated UHF oscillator, divided for VHF output.
(3) A modulator section, which accepts audio and video inputs, then uses them to modulate the UHF/VHF carrier.

**Figure:** Phase-Locked Loop Block Diagram (Source: Motorola)

**Graphic Controller: Intel 82810**

This specific graphics controller by Intel is primary product features include Processor/Host bus support, integrated DRAM controller, integrated graphics controller, 3D graphic visual enhancements, 3D graphic texture enhancements, digital video output, display, 2D graphics, Arithmetic Stretch Blitter Video, integrated graphics memory controller, display cache interface, arbitration scheme and concurrency, data buffering, power management functions, supporting I/O bridge and packaging/power. It will act as the interface in between the MPEG-2 decoder, NTSC/PAL decoder, Video ADC, NTSC/PAL Encoder, Video DACs and Color Spacer. Its block diagram is provided:
**NTSC/PAL Decoder: Texas Instruments TVP5145PFP**

This is a single-chip digital video decoder that converts baseband analog NTSC, PAL, and SECAM video into digital component video. It supports analog component, composite, and S-video inputs are supported. “Line-locked sampling is square-pixel or ITU-R BT.601 (27 MHz). The output formats can be 20-/16-bit or 10-/8-bit 4:2:2, or 10-/8-bit ITU-R BT.656 with embedded synchronization. The TVP5145 device utilizes Texas Instruments’ patented technology for locking to weak, noisy, or unstable signals, and a chroma frequency control output is generated for synchronizing downstream video encoders.

**NTSC/PAL Encoder: Texas Instruments TYP6000C**
Reverses the actions of the NTSC/PAL Decoder.

**Power Management: Texas Instruments TPPM0302**

The power manager is a low-dropout regulator with auxiliary power management that provides a constant 3.3-V supply at the output with the capability of driving a 400-mA load. It will provide a regulated power output for the STB, since it has multi input sources and would require a constant voltages source with a low-dropout voltage.

**SDRAM: Micron Technologies MT48LC128M4A2**

SDRAM is needed to support the MPEG2 Decoder and Demux. Four Micron Technologies 512 MB SDRAM (32 Meg X 4 banks) would suffice to store all of the tables for the Demux and also meet all other storing requirements. This RAM is fully synchronous (positive edge triggered). It has internal pipelined operation. In other words, the column address can be changed every clock cycle. This particular RAM has internal banks for hiding row access/precharge. Auto Precharge including concurrent auto precharge, self refresh and auto refresh modes are also included, which is vital for DRAM performance.

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**Operating System/System Platform**

In order to be consistent with IBM efforts of supporting Linux, a Linux based operating system to be used as the brain of this IBM-based set top box is chosen. Otherwise, Power TV’s latest operating systems for STBs would have been the best
choice. Monta Vista’s Linux Professional Edition embedded operating system and
development platform is chosen for this STB design.

**Enabling Linux**

Linux is becoming the favorite among consumer products. “Linux held 27%
share of server operating-system software sold in 2000, increasing from 24% in 1999 and
17% in 1998.” Source: International Data Corp. Since reducing costs is the primary
goal of manufacturers, they consider Linux as an alternate to currently available
proprietary operating systems. As Linux become more and more popular, an increased
number of applications will be developed.

**Linux Advantages**

Between 1999 and 2005, Linux’s Compound Annual Growth Rate will be in the
order of 50%. It is very easy to integrate, reliable, and stable making it extremely
attractive to developers. Its kernel requires minute memory space and best of all it is an
open-source code, which issues designer with flexibility to designers since products can
be created on various platforms. This means that many developers will continually
improve the operating system code.

The open source drivers may be leveraged and thus issuing additional cost
savings. Prior to Linux, non-recoverable expenses, per copy charges for a proprietary
operating system, and associated device drivers were being paid. With Linux, set-top box
manufacturers can use Linux as a leverage for open source drivers at no cost. From the
internet and the numerous applications point of view, Linux will also provide Internet
plug-ins and applications such as web browsers and media players. In addition, there are
not any licenses’ issues with Linux; it may be openly shared within a company.
Development Tools and Support

At one time there was a lack of Linux support on an enterprise level; companies exist now that will provide support and help developers in their everyday issues.

Conclusion

In summary, Linux provides 100% open source technology, no run-time royalties, unrestricted and free access to source code, completely open source OS and open APIs, and no dependence on single sources for proprietary technology. While other operating systems will continue to be available, designers now have an additional choice as they develop their future products. A summary of Linux’s features is given below. [2]

Highlights

- Linux 2.4 Kernel
- Linux, Solarix and VMWare hosts
- CPU support for x86/IA-32, Power PC, StrongARM, XScale, MIPS, SH, ARM, and Xtensa*
- Supports 80 + Reference and COTS Boards
- Development and configuration tools
- MontaVista Preemptible Kernel
- MontaVista Real-Time Scheduler
- Rich Networking
- Develop Integrated Development environment
- Legacy VxWorks and pSOS emulation/porting tools

Cross Development Hosts

- Red Hat 7.2, 7.3
- Yellow Dog (Mac or other PPC)
- Solarix 7.0, 8.0 (SPARC)
- SuSE 7.3
- Mandrake 8.1
- Windows NT/2000 with VMWare 3.0
Middleware will be used in this design. It is used to isolate set-top application programs from the details of the hardware and the network. This would allow application’s to operate transparently across the network without concern of anything else. Thus, the complexity of development is reduced because applications can be written to take advantage of a common API.

Presentation and application virtual machines will be put in place to avoid the recreation of content specifically for proprietary platforms. The virtual machine will act as a self-contained environment that behaves as if it is a separate STB. Thus, enabling it to serve as the run-time environment for interactive STB applications. This will allow programmers to develop STB applications independent of the actual hardware architecture used.

The present urge to converge computers, communications and entertainment is motivating cable, telecommunications, hardware and software companies to flock to set-top box deployment, which is considered the “new future gateway to the home.” This raises several questions; the ease of competing services; standards for interoperability; the freedom to purchase devices.

On-line services, banking, home security, telephony, interactive video are what is integrated into STBs. An STB’s purpose is moving towards a one-stop solution for all household needs. Distributing media like cable, telephone lines and satellite dishes to be
integrated and creating connectivity at the same time is the future. “The set-top box will support the ‘intelligent agents’ that guides users through the maze of choices. The set-top industry may itself develop into a mediating force as technology and rules governing interconnection develop. This race to define the personality and functionality of future STBs has begun. [4]

Time to market is a critical topic when it comes to STBs. Companies with the most effective Rapid Development Lifecycles methodology will win the market. This comes with one constraint of course -- Cost! This is a cost sensitive area. You can pump the largest number of STBs out, but with what price? There has to be some balance between time to market and expense. It will not be effective if a company’s set-top box is in stores the quickest, but cost much more than its competitor’s. On the other hand, it does not make sense to have the least development cost but with the longest time to market. There must be some balance.

References