Split-Drain Magnetic Field-Effect Transistor Channel Charge Trapping and Stress Induced Sensitivity Deterioration

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This paper proposed an analytical model on the deterioration of magnetic sensitivity of sectorial split-drain magnetic field-effect transistors (SD-MAGFETs). The deterioration is governed by the trap fill rate at the channel boundary traps, which is geometric dependent. Experimental results are presented which show good consistency with the analytical derivation. The deterioration is the most severe at a sector angle of 54.6°, which shows a design tradeoff with sensing hysteresis. Design guidelines for sectorial SD-MAGFET to obtain high sensitivity hysteresis and slow sensitivity deterioration are also presented which provide important information for efficient design.

***Index Terms*—Magnetic field-effect transistor (MAGFET), sectorial, sensitivity, sensitivity deterioration, split-drain.**

I. Introduction

A SPLIT-DRAIN magnetic field effect transistor (SD-MAGFET) is a common magnetic sensor, due to its simple structure, and easy integration into standard CMOS process [1]. When a properly biased SD-MAGFET is exposed to an external magnetic field orthogonal to its channel, the Hall effect will induce the Lorentz force on the charge carriers in the channel, such that the electrons flowing in the channel will be deflected and cause drain currents imbalance, also known as the Hall current, ΔI_H. The SD-MAGFET can be fabricated in different shapes [2]–[4]. The sensitivity, noise immunity, transient hysteresis of the sectorial SD-MAGFET have been investigated in literature and were found to be dependent on the geometric factors, biasing conditions and fabrication materials [3]–[6]. It is the purpose of this paper to study and analyze the boundary interface charge trapping property of sectorial SD-MAGFET through analyzing the magnetic field stressing property of the device. We shall also discuss the effects of interface charge traps on the deterioration of magnetic sensitivity in sectorial SD-MAGFET.

Shown in Fig. 1 is the layout of the N-Channel sectorial SD-MAGFET, which consists of a source terminal (Source) and two drain terminals (Drain 1 and Drain 2). Note that the gray contrast is used to identify the channel area and the source/drain areas in the SD-MAGFET. The radius of the source terminal, the channel length, the channel width between the source and the drain terminals, the spacing between the two drain terminals, the drain channel overlap, and the angle sustained by the sectorial SD-MAGFET are denoted as R, L, W, d, u, and α, respectively. When a magnetic field B_Z is applied perpendicularly to the channel (as indicated by the cross in Fig. 1), the magnetic field will induce a Lorentz force that deflects the electrons in the channel from reaching Drain 2 to Drain 1, and thus creates a differential current known as the Hall current [1] given by $\Delta I_H = I_{DS1} - I_{DS2}$, where I_{DS1} and I_{DS2} are the drain currents measured at Drain 1 and Drain 2, respectively. The sensitivity of the SD-MAGFET is defined to be [1]

$$S = \frac{1}{I_{DS}} \times \frac{\Delta I_H}{B_Z} \tag{1}$$

where I_{DS} is the total drain current (i.e., $I_{DS1} + I_{DS2}$) when no magnetic field is applied.

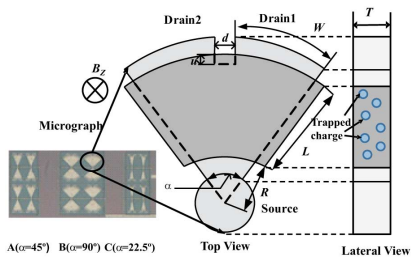

Fig. 1. Structure of the SD-MAGFETs. Micrograph, top and lateral view of the layout of the sectorial SD-MAGFET with sector angle α, channel length L, channel width W, source radius R, drain separation d, and drain channel overlapping u, where the source/drain region and channel region are in light gray and dark gray, respectively. Magnetic field is perpendicular to the SD-MAGFET channel.

When the carriers in the SD-MAGFET channel are deflected sideways by the magnetic field, they not only generate differential Hall current ΔI_H, there are also chances that they may get trapped in the channel boundary interface states and affect the performance of the device. One of the common methods to extract the channel boundary interface trap information of a MOSFET is to measure the decay in drain current of the MOSFET upon bias-induced stressing [7]–[10], which will be adopted in this work to demonstrate the existence of the channel boundary interface traps. The rest of the paper is organized as follows. Section II describes the sectorial SD-MAGFET bias-induced and magnetic field-induced drain current decay experiment. The results can be used to investigate the channel boundary interface trap. At the same time, the results will reveal the mechanism of magnetic sensitivity deterioration and its relationship with the geometry of the sectorial SD-MAGFET.

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This is because the $\Delta I_H/I_{DS}$ term in (1) is highly dependent on the property of the drain currents. An analytical model is proposed in Section III for the time dependent magnetic sensitivity of the sectorial SD-MAGFET based on the trap assisted drain current decay model in [7]. We shall also discuss the existence of an optimal sectorial SD-MAGFET layout that achieves a minimal magnetic sensitivity deterioration. Finally, the conclusion will be drawn in Section IV.

II. Experiment

The same sectorial SD-MAGFET samples and similar experimental setup have been presented in [6] and [11] for the study of transient hysteresis, and saturated magnetic field sensitivity, respectively, which will be described again in this section for the purpose of self-containment. Three samples with different geometric parameters were fabricated using a commercial $2.25\ \mu$m Metal Gate CMOS process provided by Founder Microelectronics International Corporation Limited, where the micrograph of the fabricated devices are shown in Fig. 1. To mitigate the adverse effect of layout mismatch and measurement noise, eight sectorial SD-MAGFETs with the same geometric parameters as listed in Table I were cross-couple connected to form an equivalent sectorial SD-MAGFET, such that the measured ΔI_H will be larger than the minimum measurement limit of our equipment. The channel lengths of the three samples are the same whereas their channel width varies with varying α. Fig. 2 shows the characterization circuit for the sectorial SD-MAGFET in this experiment, which consists of a pair of off-chip resistors R_1 and R_2 connecting to Drain 1 and Drain 2 of the sectorial SD-MAGFET, respectively. The resistance of R_1 and R_2 is chosen to be larger than 100 KΩ, such that large enough voltage difference is induced by ΔI_H. The R_1 and R_2 are further chosen to compensate the layout mismatch problem of the sectorial SD-MAGFET, to achieve zero differential voltage to be measured on the drains of the sectorial SD-MAGFET when it is not exposed to any external magnetic field. A supply voltage of 2.7 V and a gate voltage of 1.4 V were applied to bias the sectorial SD-MAGFET (where the typical threshold voltage, V_{th}, of the SD-MAGFET is 0.6 V) to work in saturation mode at room temperature (25 °C). Experimental results showed that ΔI_H will reduce dramatically with V_{GS} smaller than 1.4 V, while only a very small increment in ΔI_H is observed with V_{GS} greater than 1.4 V. Therefore, V_{GS} equals 1.4 V is applied in all of the following experiments. The magnetic sensitivity of the sectorial SD-MAGFETs are measured by stressing the samples under a uniform magnetic field applied perpendicularly to the sectorial SD-MAGFET channel, which is generated by an electromagnet (Lakeshore EM7-HV). Each sample is stressed for 3600 s with the above stated biasing condition, at magnetic field strength of 8000 G, 10000 G, 12000 G, 14000 G, 15000 G, 16000 G, 18000 G, and 21000 G. The variation of V_{DS1} and V_{DS2} were sampled using HP54645A Oscilloscope. By subtracting V_{DS1} and V_{DS2} from the supply voltage and dividing the results by the resistance of R_1 and R_2, respectively, we shall obtain I_{DS1} and I_{DS2}, hence ΔI_H.

III. Results and Discussions

Shown in Fig. 3(a)–(c) are plots of the normalized Hall current with respect to the corresponding span of change of each sectorial SD-MAGFET under test, such that the plots will show the relation of the Hall current variations versus geometric factors and magnetic field strengths more vividly. The experimental data obtained from sectorial SD-MAGFET with α equals 22.5°, 45°, and 90° under a magnetic field strength of 15 000 G, 18 000 G, and 21 000 G stressed for 3600 s and are plotted in Fig. 3(a)–(c), while the lines in the same figures are obtained from the proposed analytical model. Further note that the experimental data are obtained from three different sets of experiments with the same set up. It can be observed that the data sets follow the stretched exponential decay function used to describe channel boundary charge tapping [7]. Due to the difference in geometric factors and the choice of R_1 and R_2 for zero differential drain voltages, the exponential decay rate and the asymptotic limits of the three curves are different. Therefore, $\Delta I_H(t)$ can be modeled as

$$\Delta I_H(t) = \Delta I_H(0)\exp\left[-\left(\frac{t}{R_0}\right)^{\beta}\right] + \epsilon_0 \tag{2}$$

where R_0, β, ϵ_0 are the fitting coefficients account for the charge trapping rate, the dispersion parameter of the barrier energy height of charge trapping, and the intrinsic current to offset the device mismatch, measurement error and noise, respectively. Note that $\Delta I_H(0)$ in (2) is the ΔI_H of the sectorial SD-MAGFET at $t = 0$, which can be obtained from [6] as

$$\Delta I_H(0) = \frac{\mu_H B_Z I_{DS1,0}\ln\left(\frac{L+R}{R}\right)A}{(\alpha+\epsilon_1)(\alpha+\epsilon_2)} \tag{3}$$

where $I_{DS1,0}$ is the current of Drain 1 of the sectorial SD-MAGFET without external magnetic field biased at saturation, and thus $I_{DS1,0}$ depends on both V_{GS} and V_{th} with variables ϵ_1 and ϵ_2 accounting for the error of using α to approximate the charge trapping density, and A is the proportional variable that accounts for the boundary charge trapping effect. The parameter A is assumed to be a constant in [6] where the time dependence of charge trapping is not considered. To

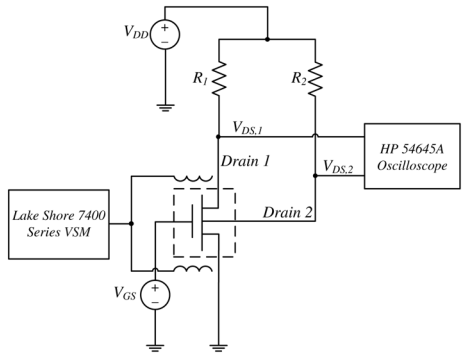

Fig. 2. Characterization circuit of sectorial SD-MAGFET, which consists of a set of off-chip balancing resistors (R_1 and R_2).

TABLE I
Geometric Parameters of Sectorial SD-MAGFETs

Sample No.	A	B	C
Channel length L (μm)	49	49	49
Radius of source R (μm)	10	10	10
Sector angle α (degree)	45	90	22.5
Drain separation d (μm)	3	3	3
Drain channel overlap u (μm)	1	1	1

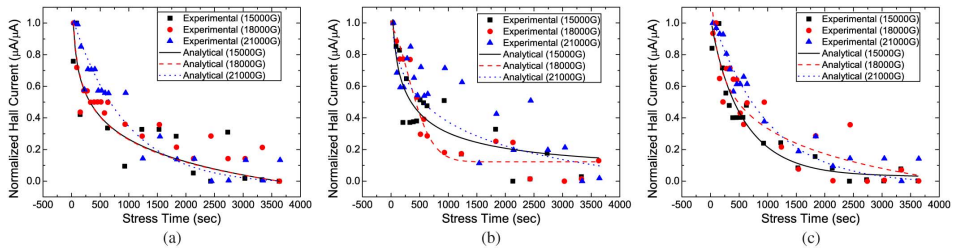

Fig 3. Plot of normalized Hall current as a function of stress time of the fabricated sectorial SD-MAGFET with sector angles (a) $\alpha = 22.5°$, (b) $\alpha = 45°$, and (c) $\alpha = 90°$, under magnetic field strength of 15 000 G, 18 000 G, and 21 000 G, where the symbols represent the experimental data and the lines represent the analytical result obtained from the proposed model depicted in (2).

TABLE II
FITTING COEFFICIENTS OF PROPOSED MODEL

$\Delta I_H(0)$	$B_Z^2/(-7.1\times10^{11}\alpha^2+7.64\times10^{13}\alpha-1.08\times10^{15})$
R_0	$1.43\times10^{8}\alpha^2-1.71\times10^{10}\alpha+5.61\times10^{11}/B_Z^2$
β	$B_Z^2/(1.63\times10^{3}\alpha^2+1.78\times10^{7}\alpha-1.59\times10^{8})$

account for the time stress experiment, we do not have fully filled or unfilled boundary interface traps, and thus the charge trapping density modeled by $A/(\alpha+\epsilon)$ will have to be modified with A being proportional to B_Z instead of a constant. Listed in Table II are the coefficients of the experimental data fitting results using the channel boundary interface trap based ΔI_H decay model in (2).

The fitting result of $\Delta I_H(0)$ (see Table II) shows that it is inversely proportional to a quadratic function of α, which is consistent with the results presented in [6]. It further reveals that $\Delta I_H(0)$ is proportional to B_Z^2. Since ΔI_H in (3) is proportional to the product of $B_Z \times A$. The parameter A is shown to be a linear function of B_Z, which is consistent with our assumption.

The parameter R_0 that determines the charge trapping rate is found to be inversely proportional to B_Z^2 and quadratically proportional to α. This observation can be explained in the same manner as the fill rate presented in [6] with the consideration of the stressing field B_Z, and thus $1/R_0$ should be proportional to $B_z \times A/(\alpha+\epsilon_1)(\alpha+\epsilon_2)$. The smaller the R_0, the higher the rate of exponential decay in $\Delta I_H(t)$ because of the higher rate of charge trapping. Due to the low energy traps at the channel boundary, the trap centers will be generated and recombined continuously until the generation and recombination rate reaches an equilibrium, where $\Delta I_H(t)$ also reaches the steady state value.

The parameter β accounts for the dispersion parameter of the barrier energy height of the channel boundary interface trap. The higher the β, the higher the activation energy required to trap the carriers, thus it leads to a longer time for the generation and recombination rate to reach the equilibrium. It is found that β is quadratically proportional to B_Z and inversely proportional to the quadratic function of α, which can be explained in a similar manner as that of R_0.

Samples of the model fitting results are plotted in Fig. 3(a)–(c) (see the lines) together with the experimental data, which shows that the model is well matched with the experimental results. The good fitting between the experimental data and the proposed model also shows that the experimental measurement, and hence the performance of the sectorial SD-MAGFET devices, is repeatable. The result reveals that the decay in ΔI_H, and hence the deterioration in the magnetic sensitivity of the

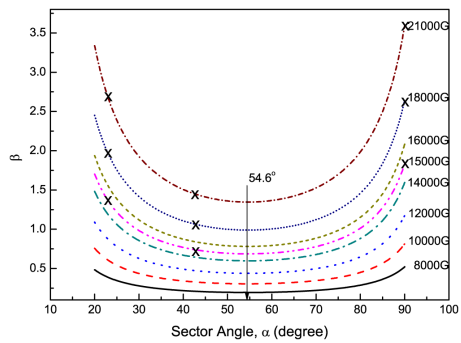

Fig. 4. Plot of fitting coefficient β as a function of sector angle α for different magnetic field strength, where crosses represent the fitting parameters obtained from experimental data.

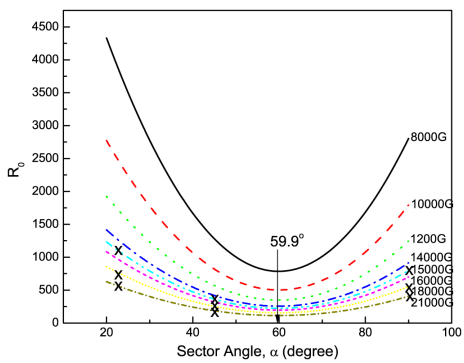

Fig. 5. Plot of fitting coefficient R_0 as a function of sector angle α for different magnetic field strength, where crosses represent the fitting parameters obtained from experimental data.

sectorial SD-MAGFET under magnetic field stress, is due to the charge trapping at the channel boundary. Consider the model fitting results, under the same magnetic field strength at 18 000 G, the device with $\alpha = 45°$ has the most rapid decay rate, in which ΔI_H takes 1300 s to reach steady state (i.e., the channel traps are fully trapped), while ΔI_H of the other two samples ($\alpha = 22.5°$ and $\alpha = 90°$) do not reach the steady state after the stressing period under 18 000 G. However, the decay rates of the Hall current with respect to magnetic field strength are observed to be similar for all three devices under the magnetic field strength of 15 000 G and 21 000 G. Hence, it shows that the rate of deterioration in magnetic sensitivity is α dependent. The deterioration is also shown to be magnetic field dependent. These dependences are best visualized by plotting the fitting parameters β and R_0 with respect to α at various magnetic field strength B_Z as shown in Figs. 4 and 5.

Fig. 4 shows the plot of parameter β as a function of α for different B_Z based on the proposed model in (2), where fairly

symmetrical curves are observed with axis of symmetry at $\alpha = 54.6°$. The crosses shown in the same figure are the fitting parameters obtained from the experimental data, which shows the good consistency of the proposed model. The symmetrical curves show that the trapped charges acquire a higher barrier height in sectorial SD-MAGFET with too small α and too large α because of the inefficient deflection of a carrier towards the sidewall of the channel boundary driven by the induced Lorentz force, which makes the ΔI_H decay slower, hence the rate of sensitivity deterioration is lower. The lowest β for different B_Z is observed at $\alpha = 54.6°$, which is shown to be consistent with α that achieves the largest magnetic sensing hysteresis in [6]. This is because the sensing hysteresis is proportional to the channel boundary charge trap fill rate, and the smaller the β, the higher the fill rate. It should be noticed that the sectorial SD-MAGFET with $\alpha = 54.6°$ will also achieve the highest sensitivity deterioration. As a result, there exists a design dilemma, where high sensing hysteresis devices are desired in sectorial SD-MAGFET applied as magnetic sensor. However, high magnetic sensing hysteresis sectorial SD-MAGFET will also have high magnetic sensitivity deterioration, and hence should be avoided for applications that require long operating time. Fig. 5 shows the plot of parameter R_0 as a function of α under different B_Z based on the proposed model in (2). The R_0 is a quadratic function of α. The crosses shown in the same figure are the fitting parameters obtained from the experimental data, which shows the good match of the proposed model. These plots show consistent symmetrical curves as those shown in Fig. 4 but the axis of symmetry is found to be at $\alpha = 59.9°$, which is consistent with the observation obtained in Fig. 4. R_0 has a similar effect at $\alpha = 59.9°$; however, the magnetic sensing hysteresis is reported to achieve its optimal at $\alpha = 56°$ [6], which implies the effect of β, i.e., the exponential factor is a dominant parameter instead of R_0 (i.e., the time that $\Delta I_H(t)$ reaches its steady state value).

To avoid the adverse effect in the sensitivity deterioration, the designer has to consider the decay rate such that the magnetic sensing operation can be completed before the ΔI_H decays to the level that is out of the detectable margin of the subsequent detection unit. In other words, the longer the decay time, the wider the operation time of the sectorial SD-MAGFET, where the decay time is proportional to β and inversely proportional to R_0, in which the β dominates the rate of sensitivity deterioration. Therefore, it is more important to consider the parameter β for the investigation of sensitivity deterioration. The designer should also consider the layout parameter α for the design tradeoff between the sensitivity deterioration, the magnetic sensitivity, and the sensing hysteresis. A possible solution to achieve high sensing hysteresis for accurate detection while alleviating the sensitivity deterioration problem is the application of power clock to drive the sectorial SD-MAGFET with $\alpha = 56°$. With appropriate duty cycle in the power clock signal, the sectorial SD-MAGFET will periodically reset and thus relieve the channel charge trapping sensing deterioration problem. The added advantage of power clocking the sectorial SD-MAGFET is the increase in power efficiency of the device. The con is the added complexity in the magnetic sensing circuit.

IV. Conclusion

The magnetic sensitivity deterioration of sectorial SD-MAGFET due to the charge trapping at the channel boundary was investigated by modeling the Hall current decay in the sectorial SD-MAGFET using stretched exponential function. The proposed model is shown to be well matched with the experimental results, where the sensitivity deterioration is mainly affected by the fill rate of the traps at the channel boundary determined by the geometric factors. The results show that the sensitivity deterioration is the most severe with sector angle $\alpha = 54.6°$ in our model, which is consistent with the $\alpha = 56°$ reported in literature to achieve the highest sensing hysteresis (a side effect of sensitivity deterioration). Our study reveals that there is a design tradeoff between magnetic sensitivity and sensitivity deterioration, in which the designer is required to balance the magnetic sensitivity and the operation time of the sectorial SD-MAGFET before the sensitivity deteriorates to an unacceptable level. Note that power clocking with an appropriate duty cycle can be applied to promote the sensitivity of the sectorial SD-MAGFET while avoiding the sensitivity deterioration problem at the cost of complex detection circuit.

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