# Carry-Select Adder

ECE 658 VLSI-I

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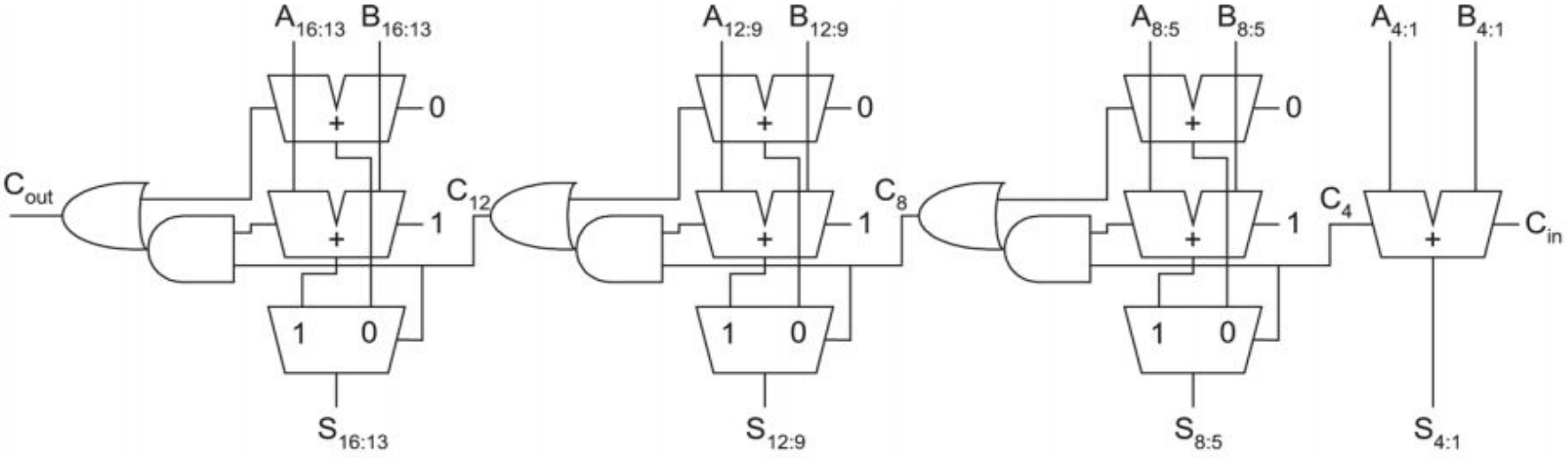
# Introduction

Design a 32-bit carry-select adder as shown in the figure utilizing the n-well 0.18 μm CMOS (SUBM) process (λ = 0.1 μm) as described in course. Use your own design approach to satisfy the requirements for the chip, which include:

- Speed: Data output rate: preferably 900 MHz if possible but definitely not less than 850MHz.
- Logic Reliability: Good Noise Margin
- Less than 40 pin-out count



# Design

**Advantages of Carry-Select Adder**

Performance is better.

**Disadvantages**

Area is increased because of the extra full adders.

# Design Challenges

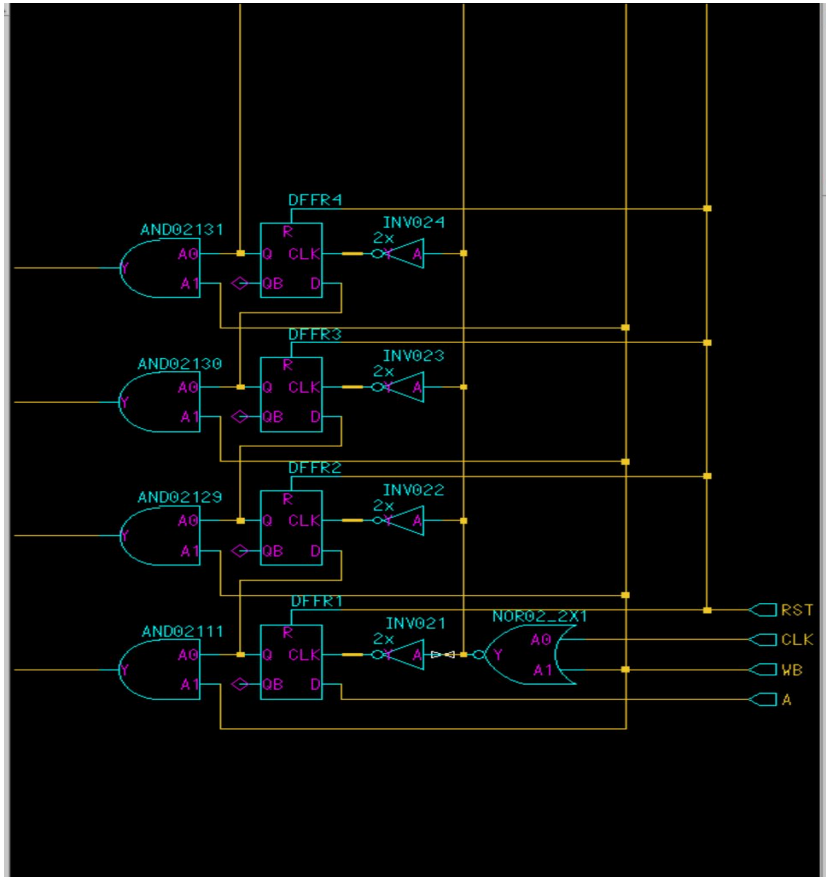
**Carry-Select Adder Design and Challenges**

- Due to limitation in input pins on the pad, we had to design Serial In Parallel Out(SIPO).
- Delay in carry propagation. We reduced delay by keeping buffers at carry out of the adders.

# Design Challenges

**SIPO Design and Challenges**

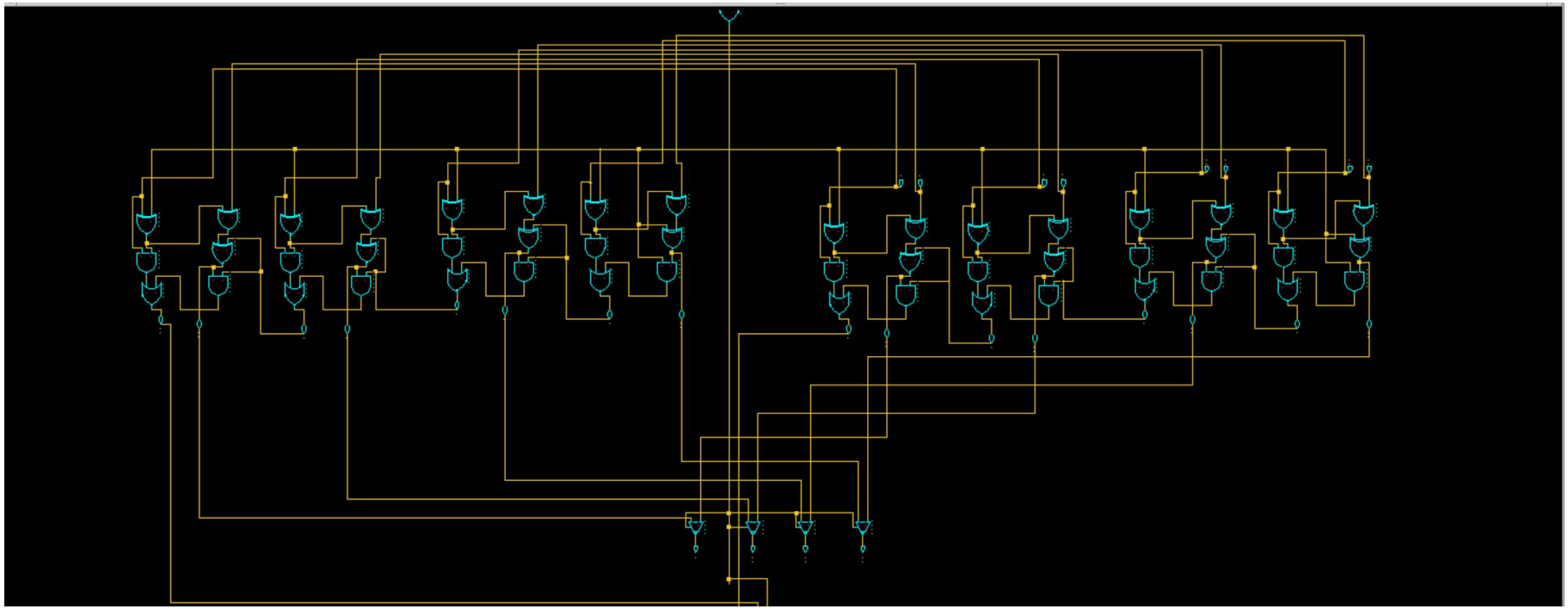
- The output of the NOR gate has a load of 32 flip flops, because of the the clk signal was degraded.
- Buffers were added at the output of the NOR gate, which solved the issue of degraded signal.
- HSpice simulation of the 32 bit SIPO was a challenge due to big waveform file



# Design Challenges

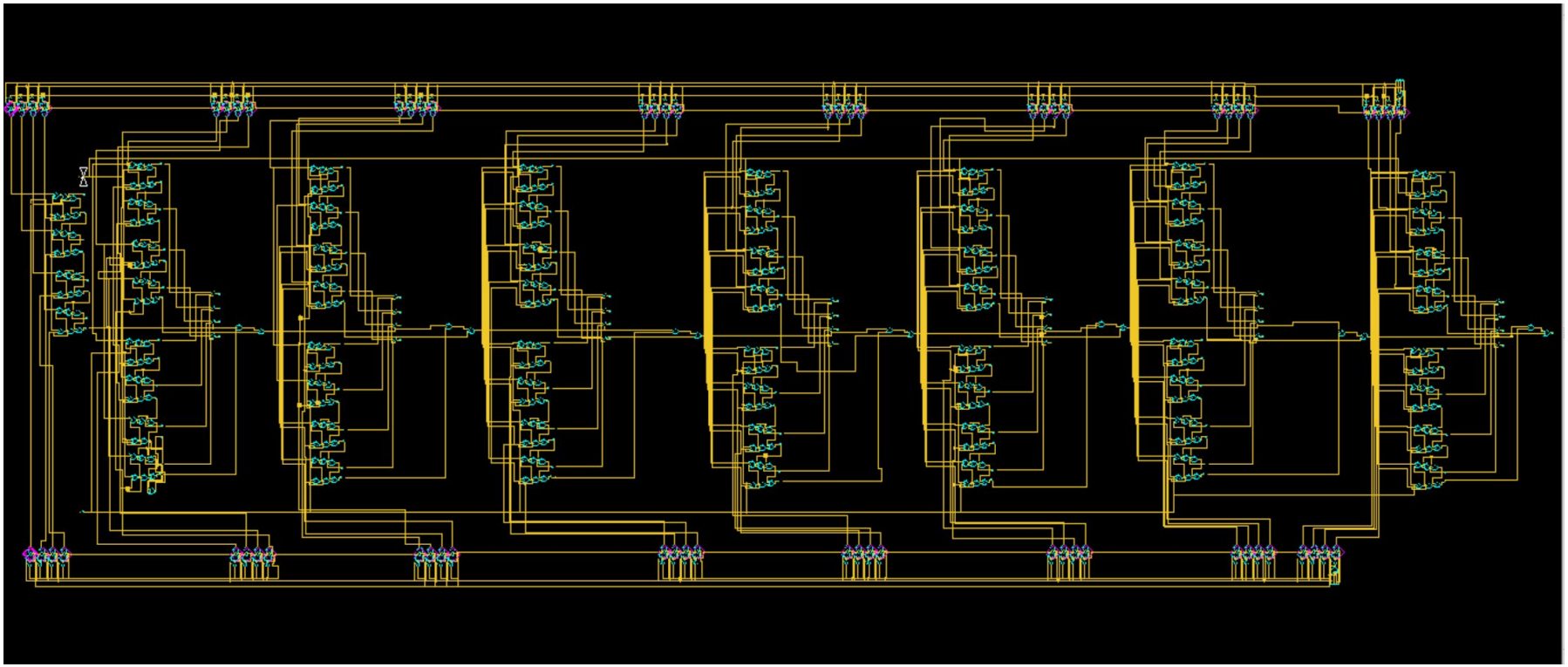
**Carry-Select adder design**

**Four-bit adder**

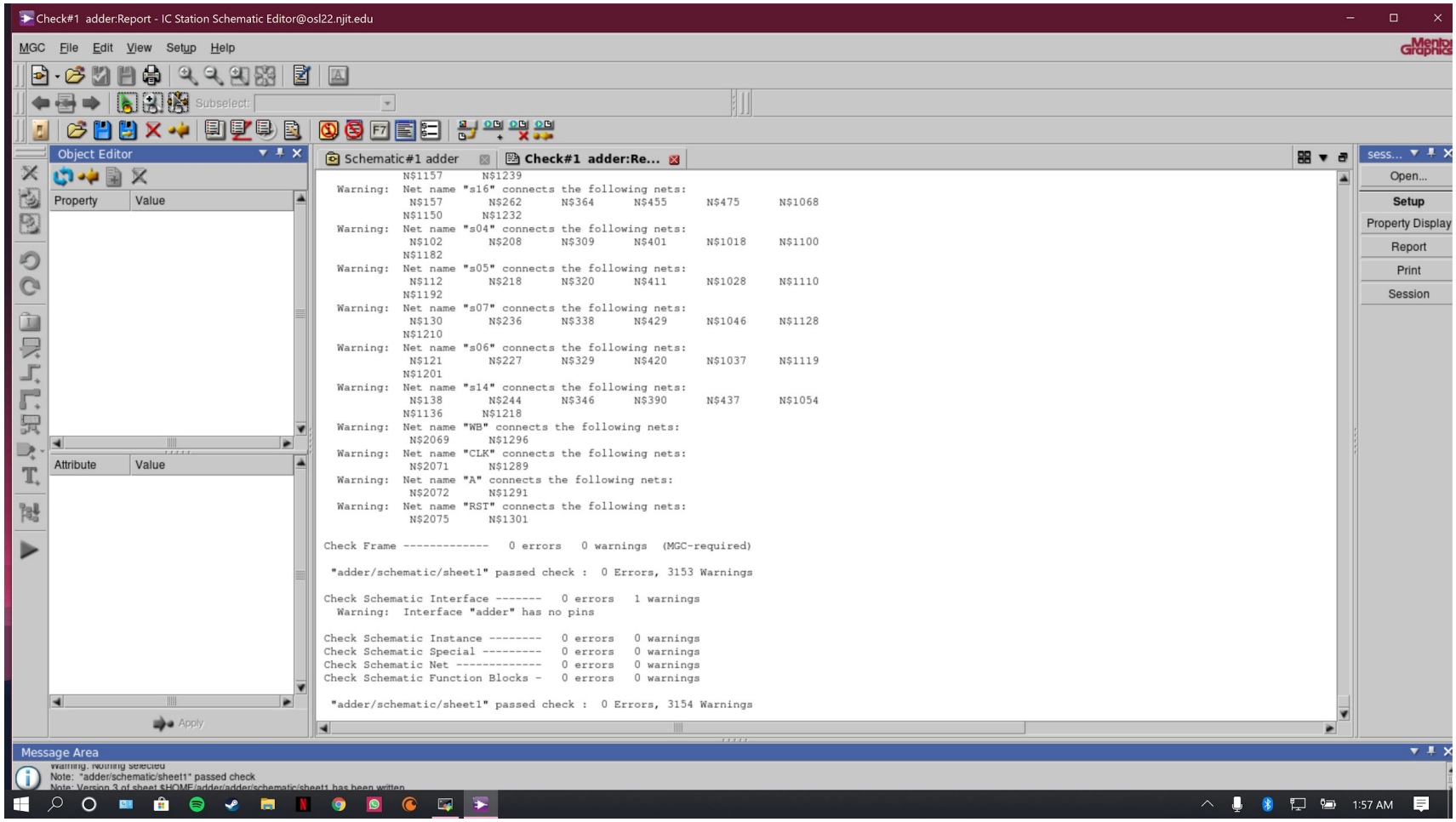


# Design Challenges

**32 bit Carry-Select adder design**

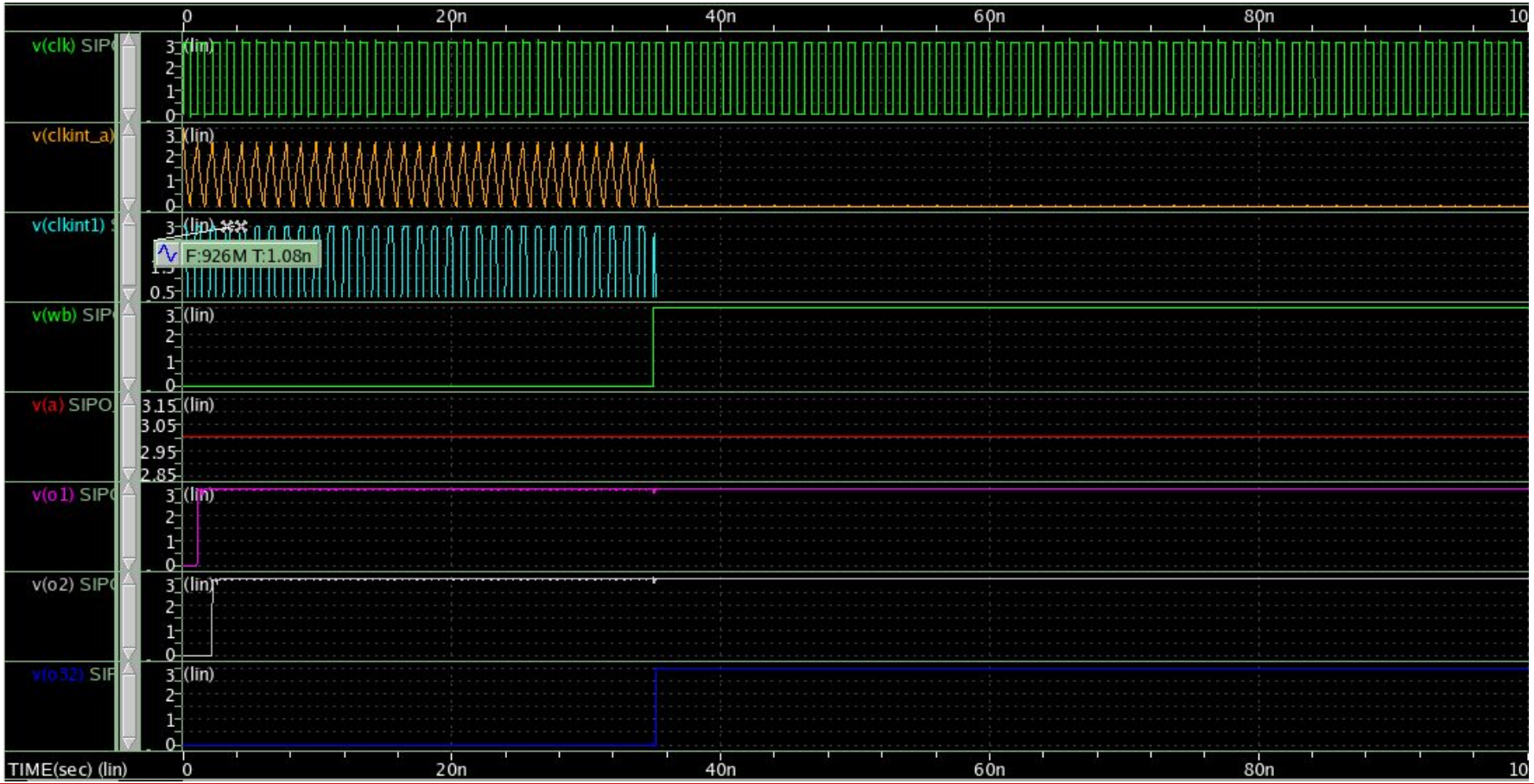


# Design Challenges



# HSpice simulation

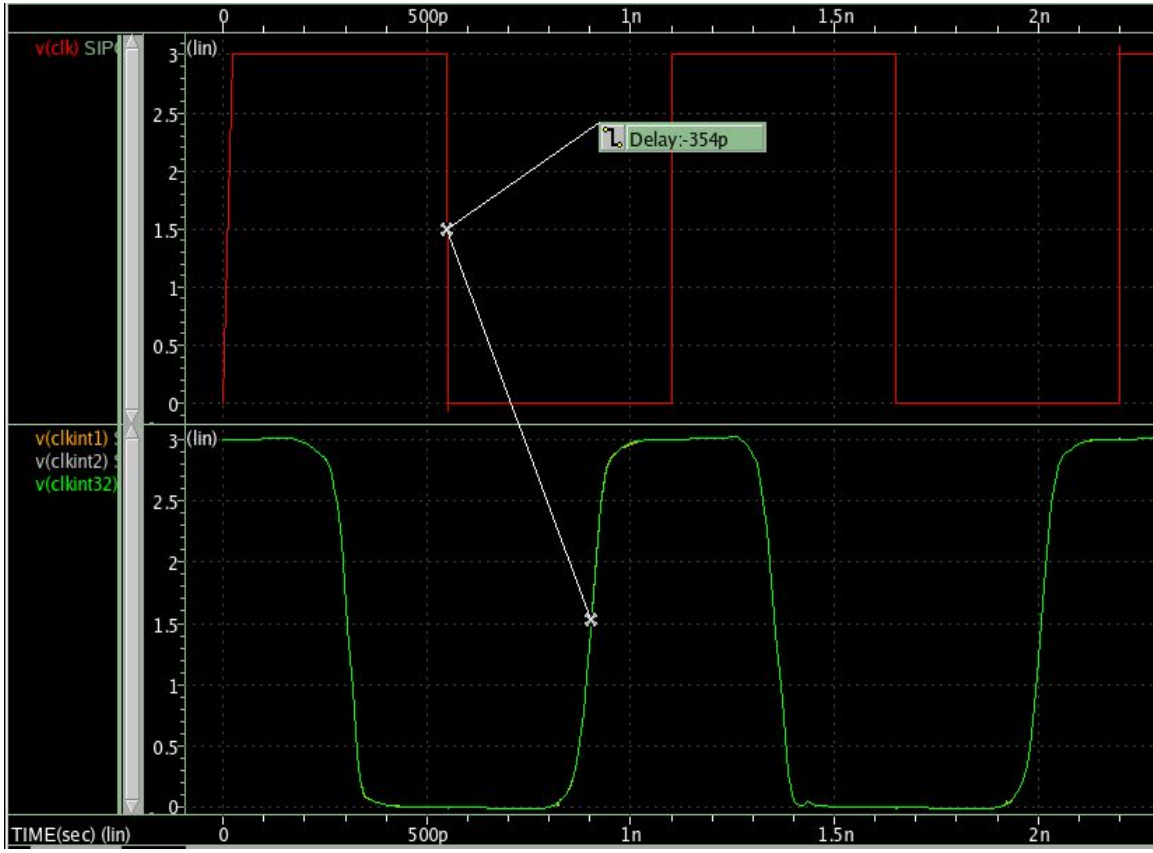
## 32-bit SIPO working



# HSpice simulation

**Clock delay**

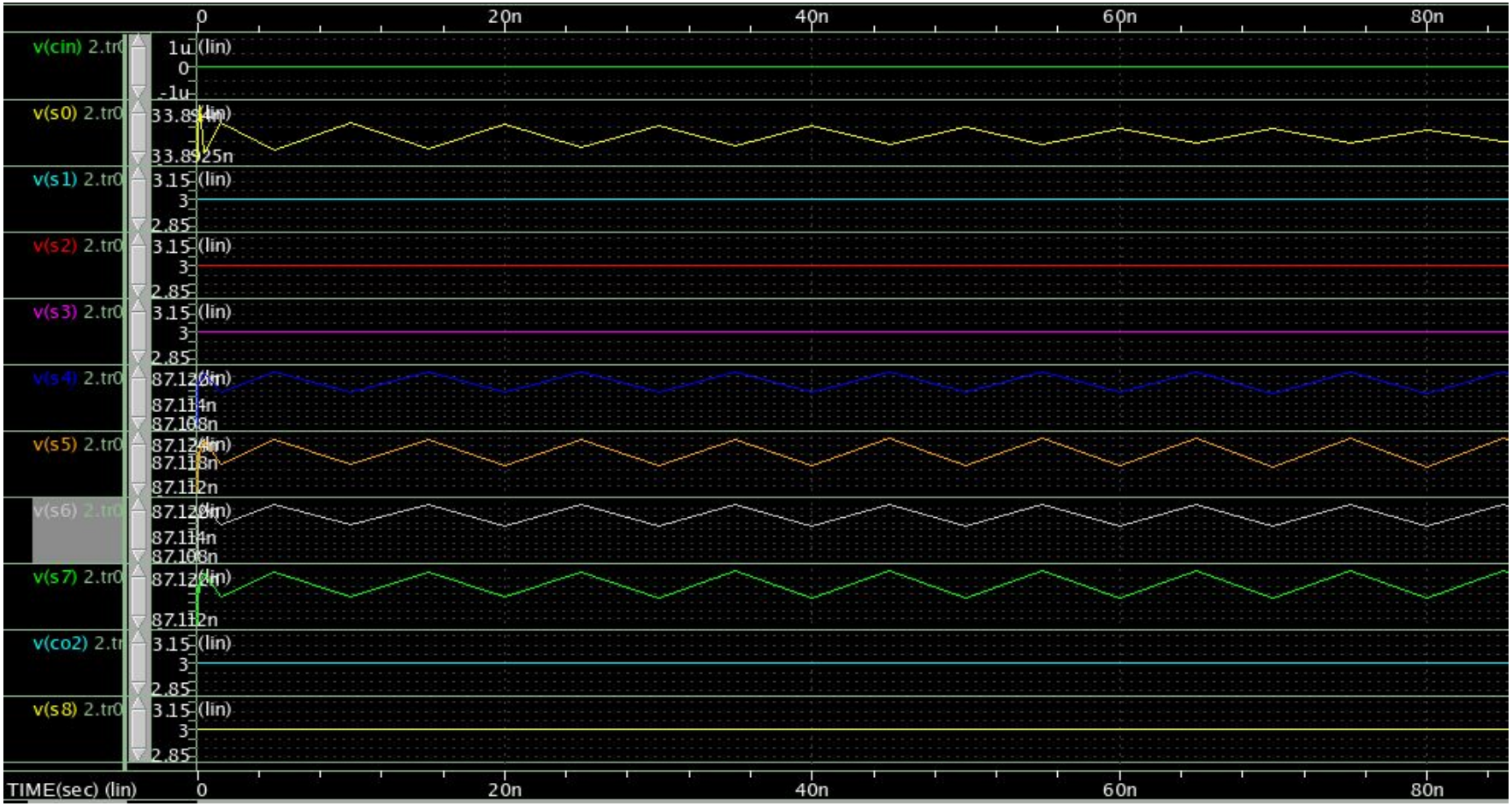
- Pex extracted gates components where used for simulation.
- Therefore, the layout capacitance were included.
- The clock delay can be reduced further



# HSpice simulation

**Carry Selecting Adder working(8_bits)**

**A=00001111 B=11111111 SUM=011100001**



# Applications

**Image processing** In image processing with interpolation, an output of the gamma circuit and the input data are input to an adder circuit so as to obtain the added and averaged values at a predetermined ratio.

**Signal processing** Addition is by far the most fundamental arithmetic operation. It has been ranked the most extensively used operation among a set of real-time digital signal processing benchmarks from application specific DSP to general purpose processors.

**Arithmetic logic units** Carry select adder is used in arithmetic logic units to perform addition and multiplication in a less amount of time.

Advanced microprocessor design In microprocessor design, the adder is used for the conversion mechanism in calculating the physical address using the offset address and segment address.

**High speed multiplications** In multiplier, each bit of the Product P is obtained by a summation of bits AiBj using an array of single bit adders. The bits AiBj are formed using AND gates.

# Further work

- Layout still needed to be done.
- Further optimisation in reduction of the clock delay for the SIPO is possible
- Optimisation for layout area still needs to be done.

# References

A.RAMESH, and B. Siva Nageswara Rao. *EFFICIENT AND ENHANCED CARRY SELECT ADDER FOR MULTIPURPOSE APPLICATIONS*. www.ijser.org/researchpaper/EFFICIENT-AND-ENHANCED-CARRY-SELECT-ADDER-FOR-MULTIPURPOSE-APPLICATIONS.pdf.

Weste, Neil H.E. CMOS VLSI design:a circuit and system perspective / Neil H.E. Weste, David Harris.--3rd ed.

# Thank you!!

Questions are welcomed!